

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG/Memory	3-5
CPU-Power,CPU-GND	6-7
DDR4 U-DIMM	8-11
PCH-LPC/HDA/RTC/MISC/SPI , PCH-Clock/Audio	12-13
PCH-DMI/PCIE/USB/SATA	14
PCH-GPIO/RSVD , POWER/GND , Strap	15-18
SPI ROM-BIOS	19
HDMI Connector	20
DVI Connector	21
VGA - RTD2166	22
PCIE SLOT-CPU(X16),(X1)	23-24
SATA CNT&M.2 Card	25-26
RUSB 3.1 G1 A+C+Redeiver	27
Rear USB3.0/2.0	28
Front USB 3.0/2.0	29
USB Power	30
LAN - I219	31
AUDIO ALC887	32
SIO-NCT6797D1/2	33-34
COM/LPT/PS2	35
CPU/PUMP FAN Type K SYSTEM FAN1/2 Type K	36-37
RGB/AUDIO/EZ DEBUG LED PCIE/AUDIO LED	38-39
CLR COMS/CUT VBAT	40
ACPI-3VSB/3VDSW	41
CURRENT SENSE-RT9553B	42
VCORE+VGT-PWM-RT3607BC	43
VCORE-MOS-PHASE 1~4	44
VGT-MOS-PHASE 1~2	45
CPU PWR-VCCSA-NB685	46
CPU PWR-VCCIO-SY8288	47
CPU PWR-VCCST/PLL	48
DDR PWR-RT8231	49
DDR PWR VPP25-MP2147/VTT	50
PCH POWER-RT8125E PCH POWER-1P8V	51-52
ATX Connector/F_Panel	53
Manual Parts	54

**MS-7B19** mATX  
Ver: 10

## Coffeelake Platform

**CPU:** Coffeelake S

**PCH:** B360

**SPI ROM : 128 MB**

**Memory:** DDR4 \* 4 (Dual Channel)

**Power Solution:**

**CPU :** RT3607

**VCCSA :** NB685

**VCCIO :** SY8288

**DDR :** RT8231

**PCH :** RT8125E

**ACPI:** MPS

**Onboard Chip:**

**LAN** RTL8111H

**Dual Codec:** ALC887

**SIO:** NTC6797

**Type C:** ASM1543

**USB3 Redrive :** ASM1464 X 1

**Expansion Slots:**

**PCI Express (X16) Slot \* 1**

**PCI Express (X1 ) Slot \* 2**

**M.2 Slot (Socket 1 ) \* 1**

**LED**

**EZ Debug LED**

**Audio Line LED**

**Rear I/O Connectors**

**PS2**

**USB2.0x2**

**USB3.1 Gen1x4**

**RJ45 + USB3.1 (Type C+ A)**

**Audio Jack 3 Port**

**HDMI+DVI+VGA)**

**Internal Connectors**

**Dual SATA \* 3**

**FUSB3.0 Header \* 1**

**FUSB2.0 Header \* 2**

**Front Audio Header \* 1**

**Front Panel Header \* 2**

**SPI Header \* 1**

**TPM Header \* 1**

**CPU Fan \* 1**

**System Fan \* 2**

**Internal Pin Header**

**JRGB1**

**JSPI1**

**JCI1**

**JBAT1**

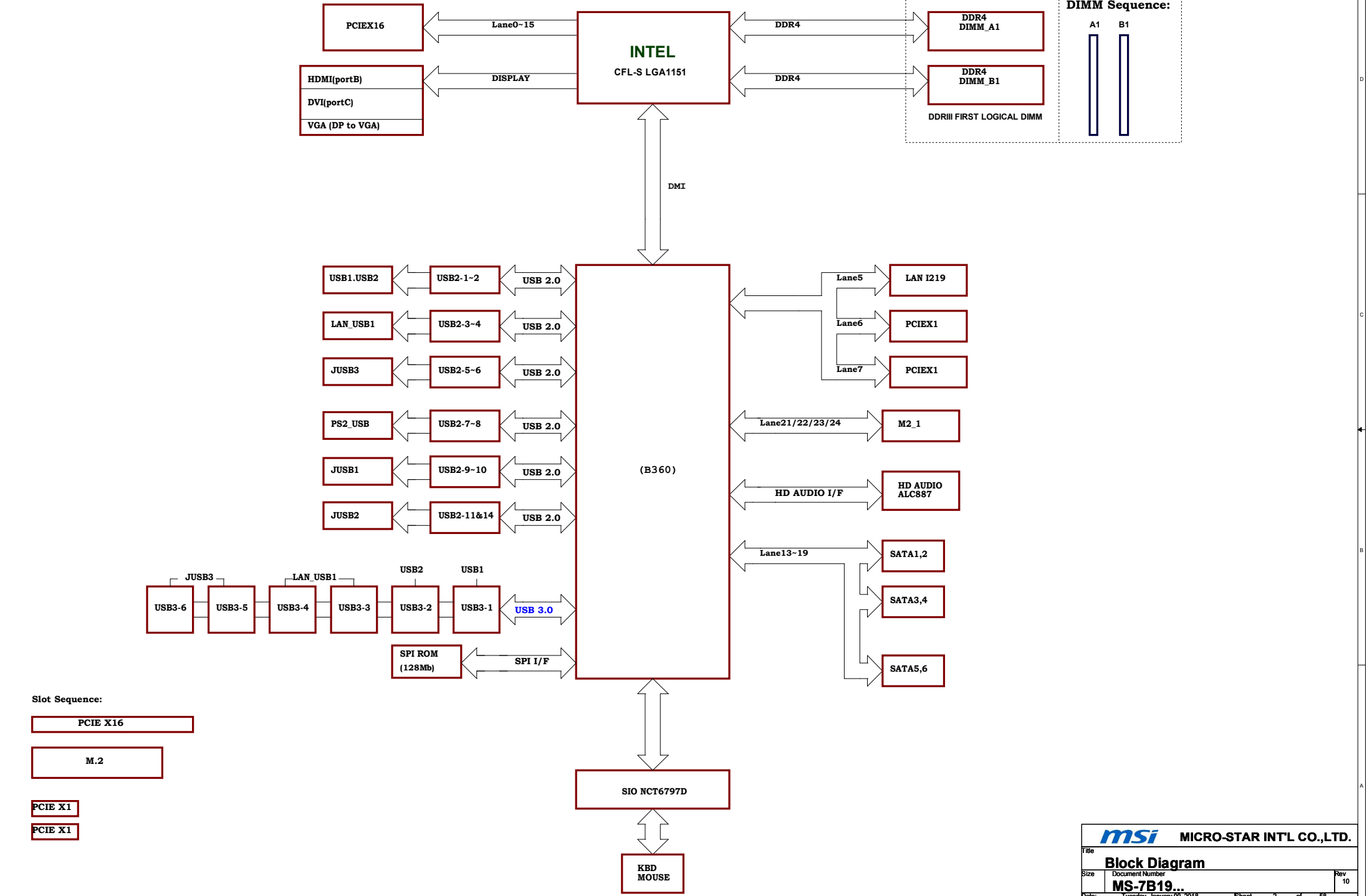
**JCOM1**

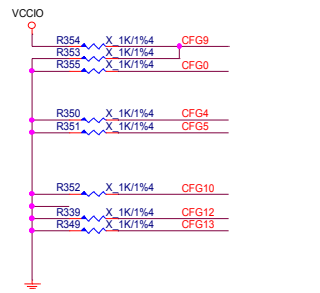
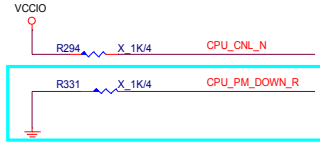
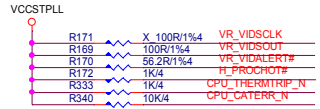
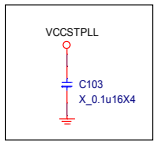
**JTPM1**

**JLPT1**

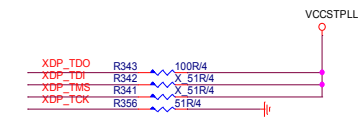
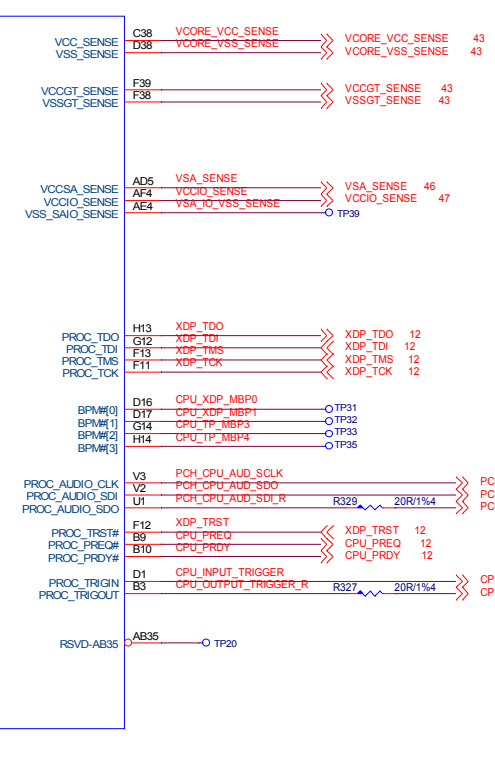
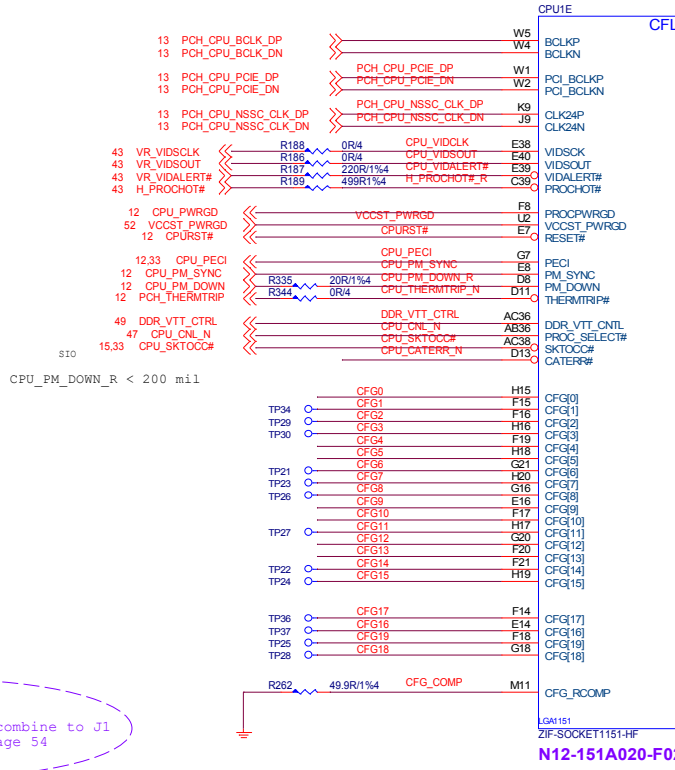
 MICRO-STAR INT'L CO.,LTD.			
Title <b>Cover Sheet</b>			
Size	Document Number	Rev	
	<b>MS-7B19...</b>	10	
Date:	Tuesday, January 09, 2018	Sheet	1 of 58

MS-7B19 Block Diagram

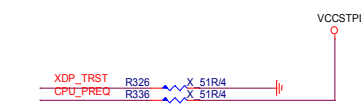




2017/7/13  
Remove JP1 because JP1 combine to J1  
Please see the D78 on page 54



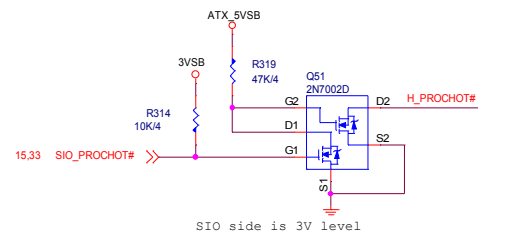
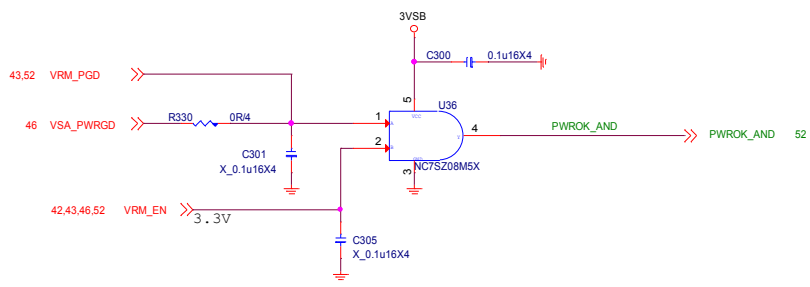
Close CPU <1100 mil  
1000 mil < CPU\_XDP\_MBP0-1 < 6000 mil



## VRM Sequence

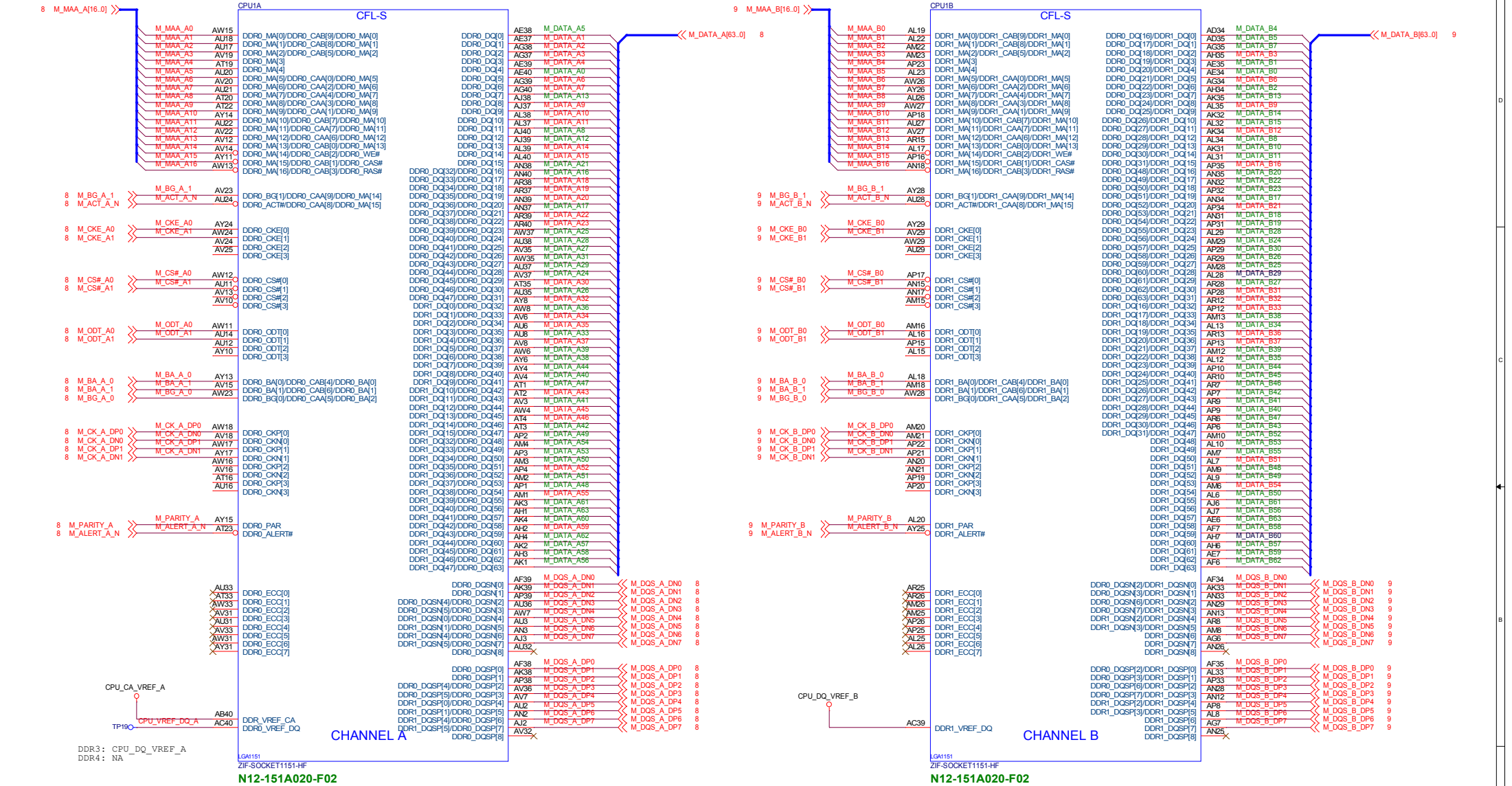
11/30 Modify for SILEGO Sequence

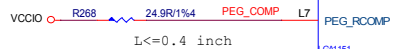
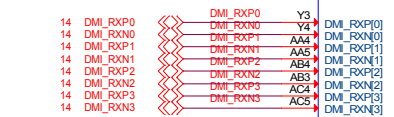
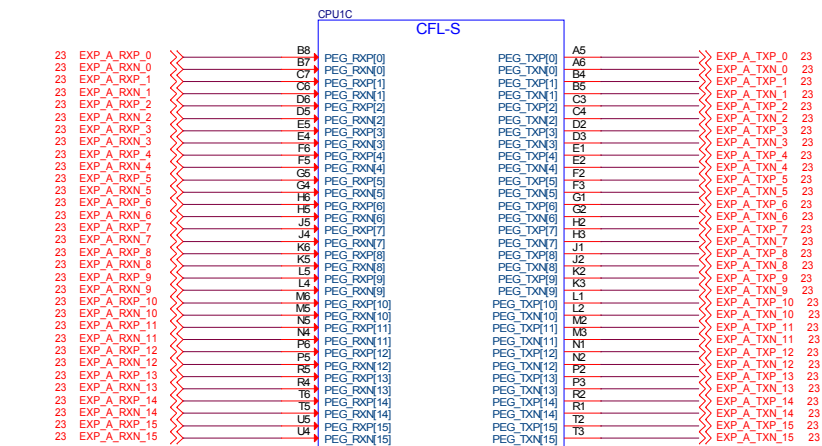
MP Remove?



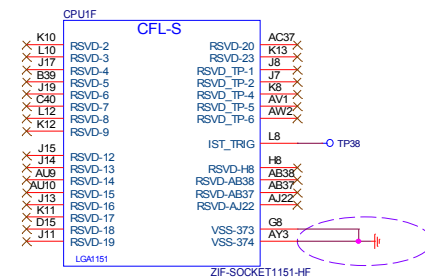
## CFG Strap

CFG Table		
HIGH	LOW	DESCRIPTION
0	No Lock	PCU PLL Lock
1		RSVD
2	NORM	PEG LANE REVERSAL
3		RSVD
4	DISABLE	ENABLE
5	DISABLE	ENABLE
6	DISABLE	ENABLE
7	RESET#	BIOS_REQ
8		RSVD
9	PRESENT	NO PRESENT
10		RSVD
11		RSVD
12		RSVD
13		RSVD
14		RSVD
15		RSVD
16		RSVD
17		RSVD
18		RSVD
19		RSVD





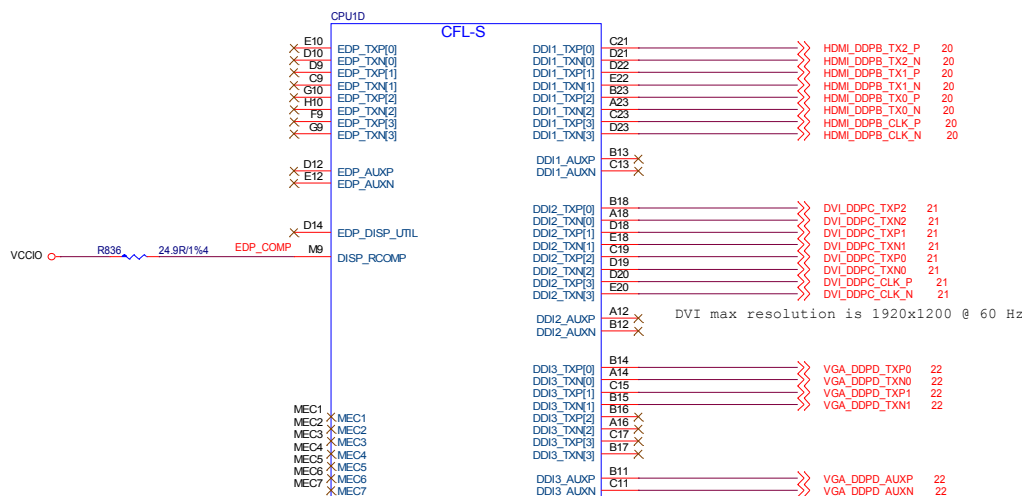
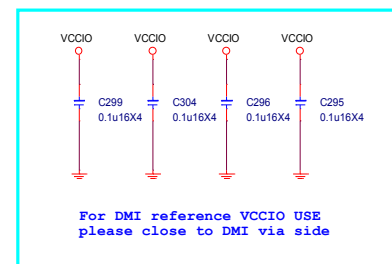
LGA1151  
ZIF-SOCKET1151-HF  
**N12-151A020-F02**



**N12-151A020-F02**

2017/7/12

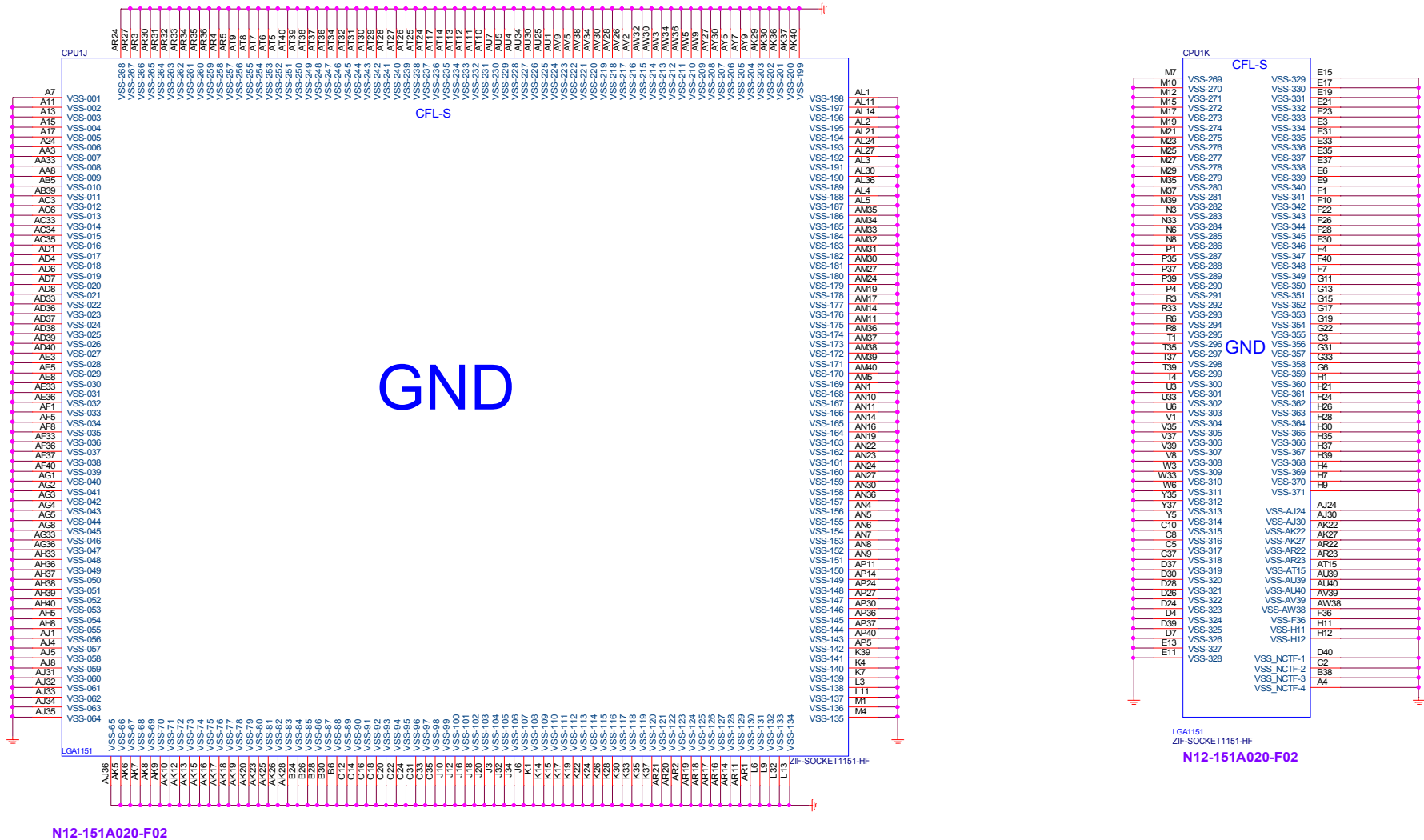
G8 and AY3 can connect directly by CRB 1.0



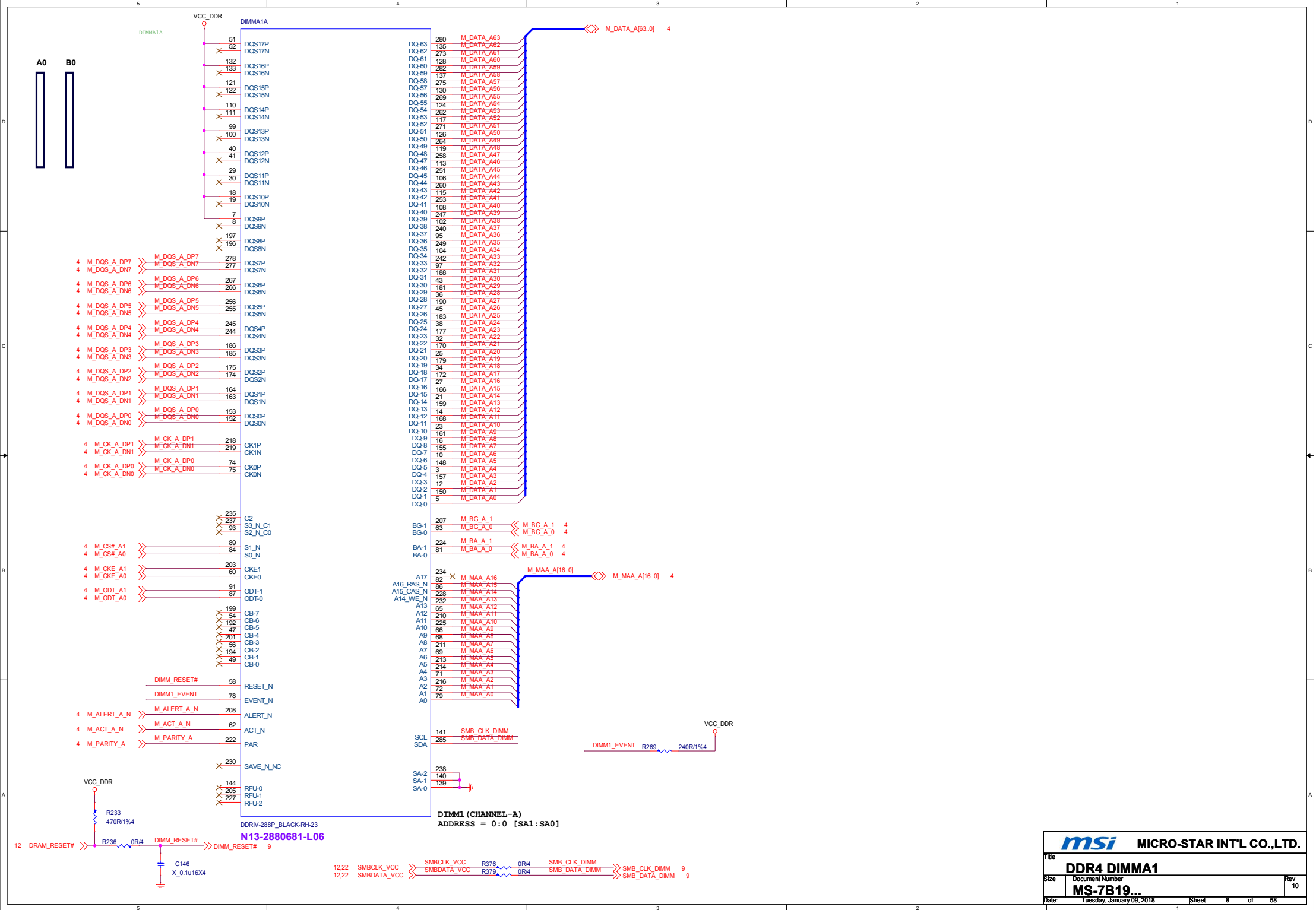
DVI max resolution is 1920x1200 @ 60 Hz

LGA1151  
ZIF-SOCKET1151-HF  
**N12-151A020-F02**



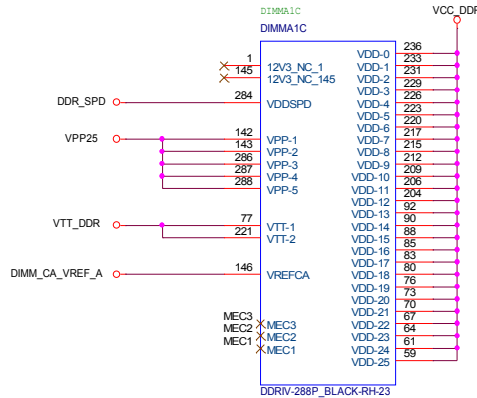




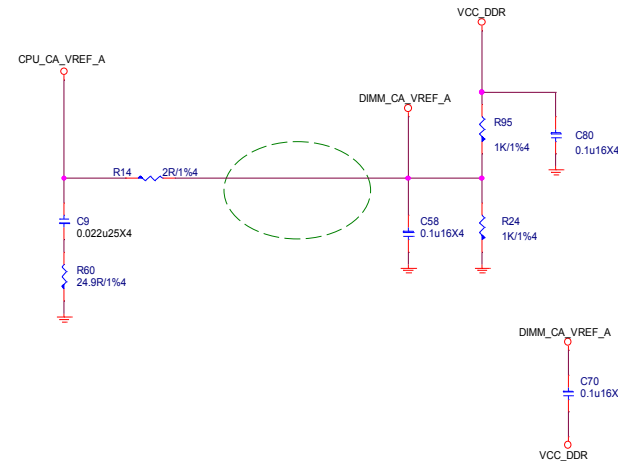
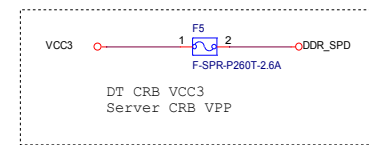
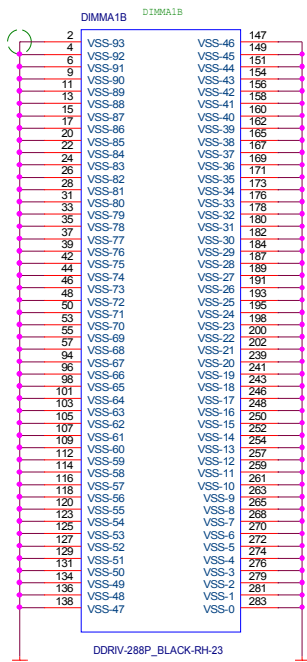
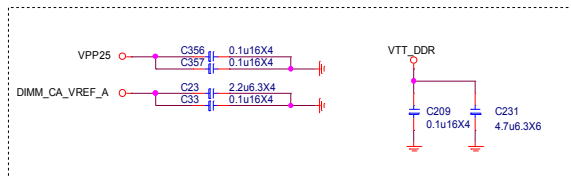
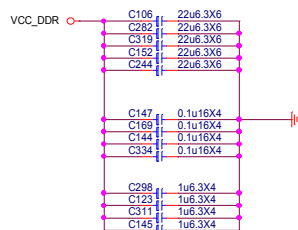
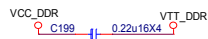
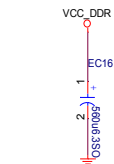


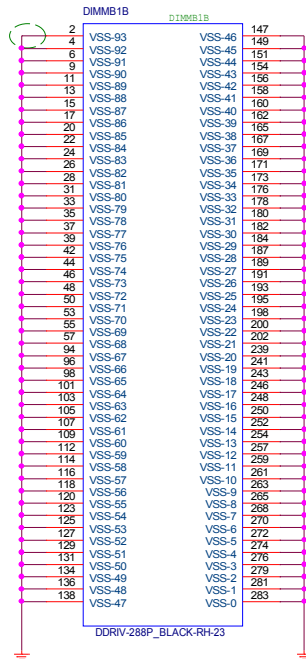
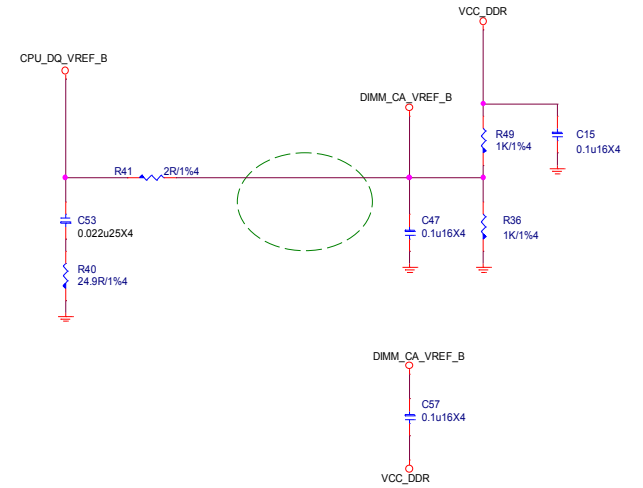
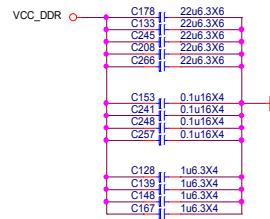
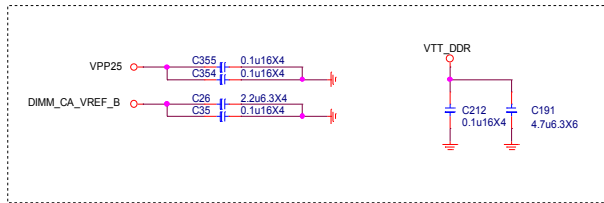
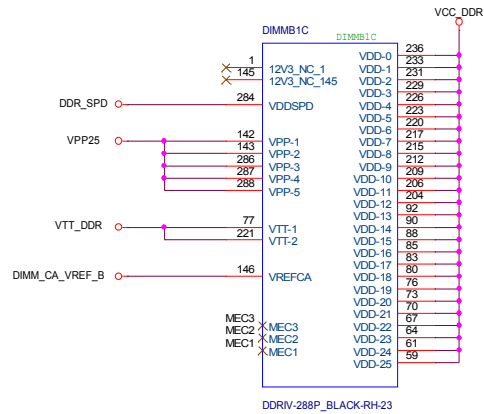


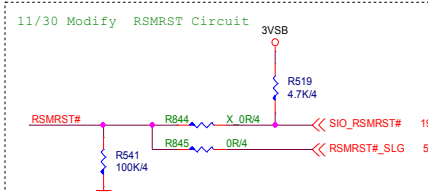




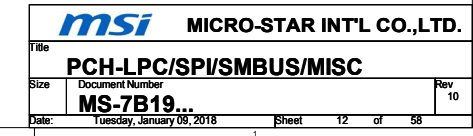
# DIMM SLOT PN BY SPEC





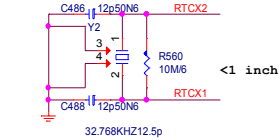


## 11/30 Modify DPWROK Circuit

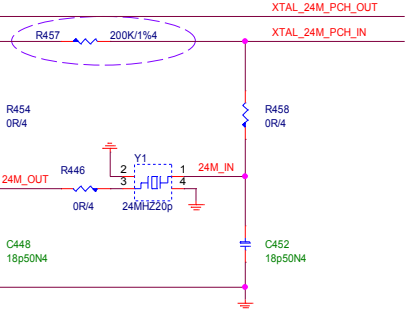


PCH\_CLK

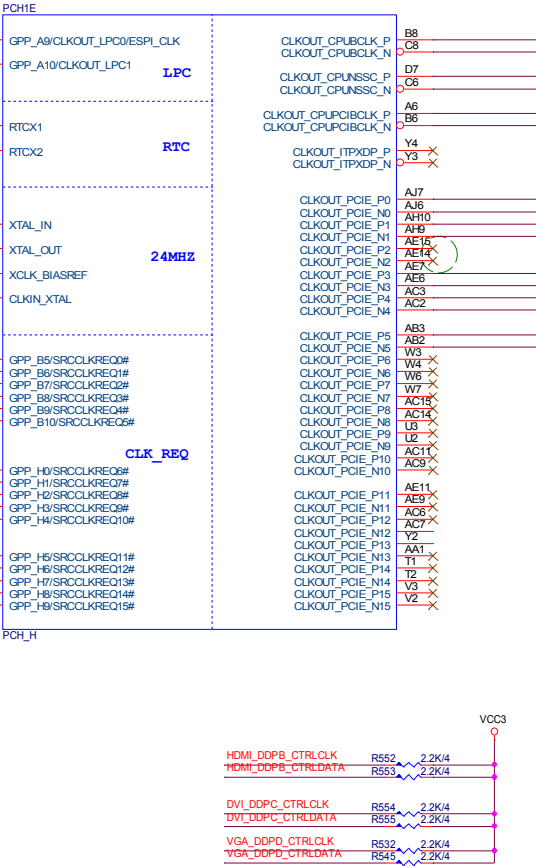
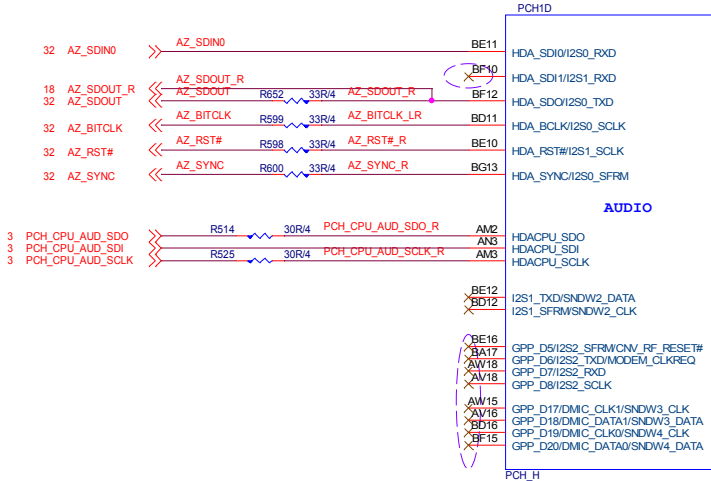
Close to PCH



2017/7/11  
The value of R689 is the same as PDG r0.9 by Intel's feedback



PCH\_AUDIO

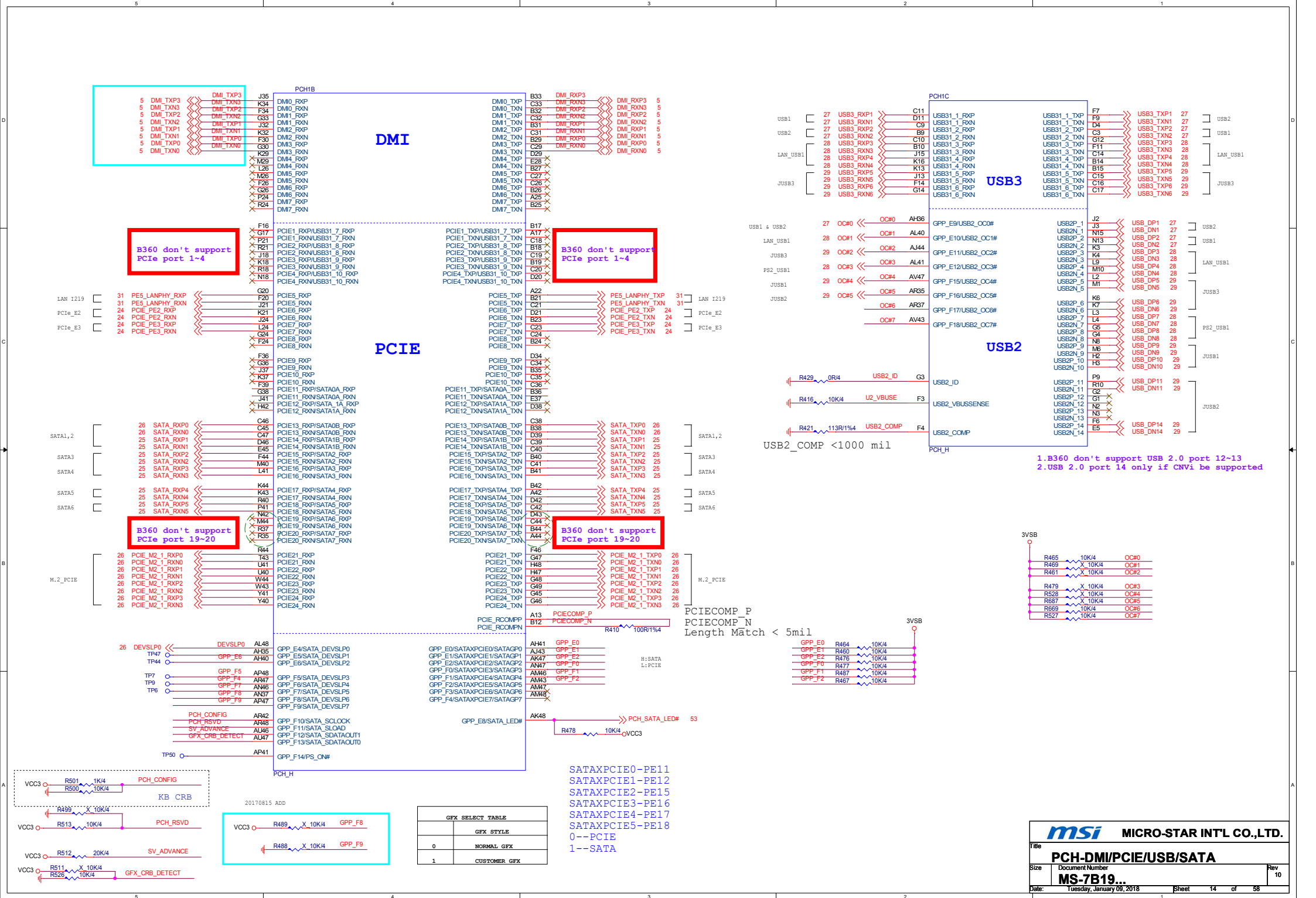


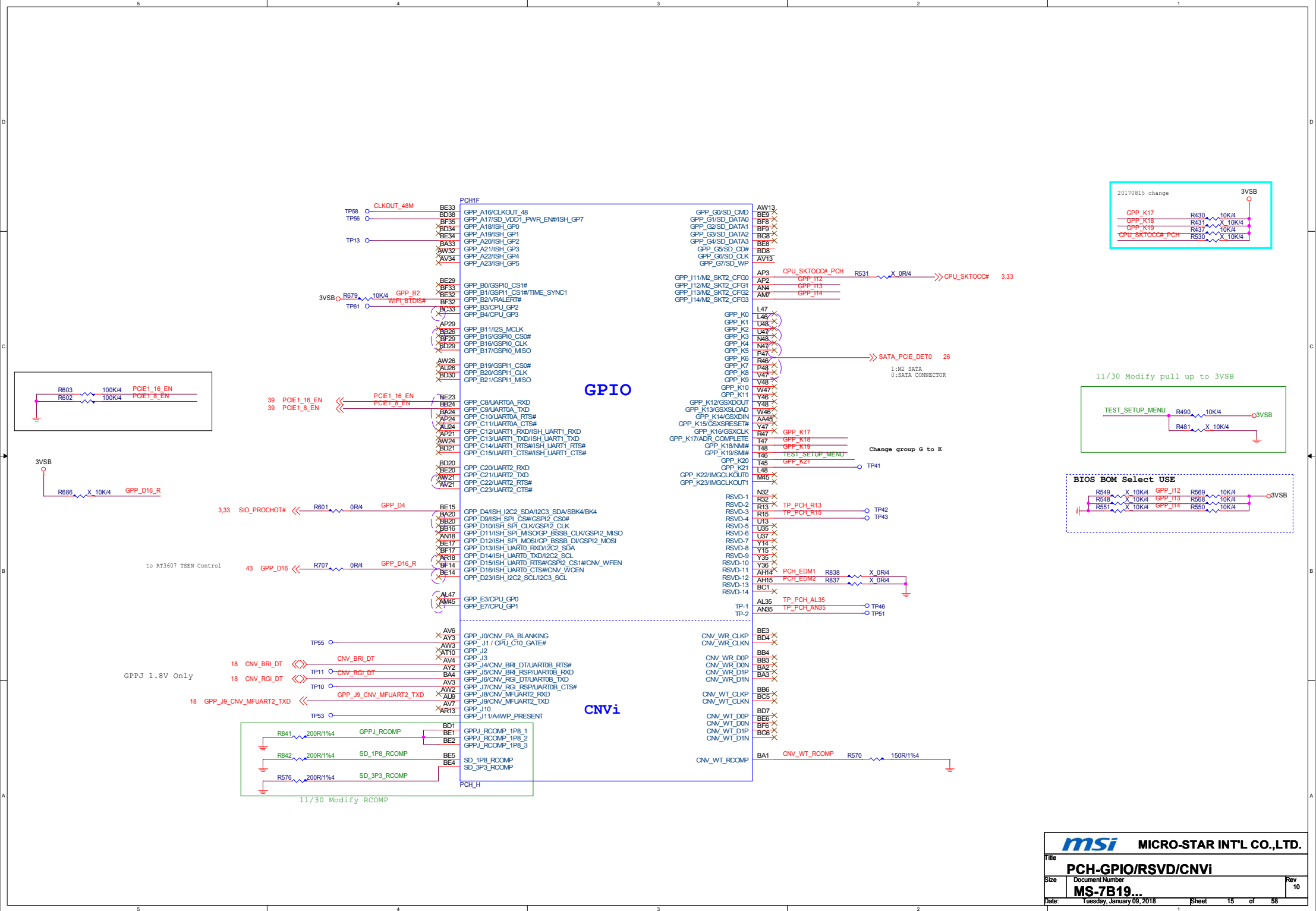
Internal pull-down is disabled after PCH\_PWROK is high.

0 : Port B is not detected. (Default)  
1 : Port B is detected.

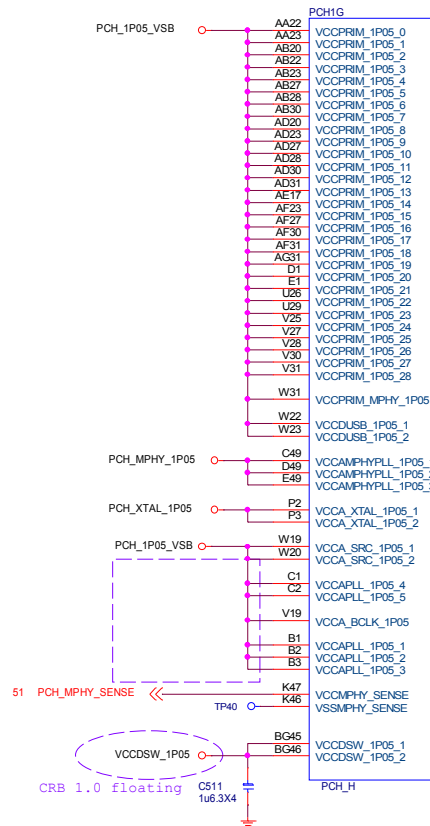
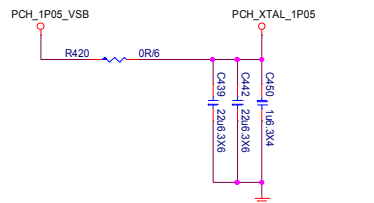
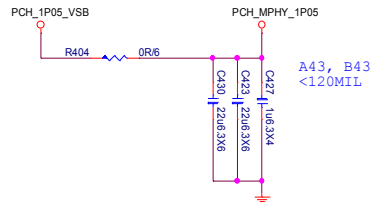
0 : Port C is not detected. (Default)  
1 : Port C is detected.

0 : Port D is not detected. (Default)  
1 : Port D is detected.

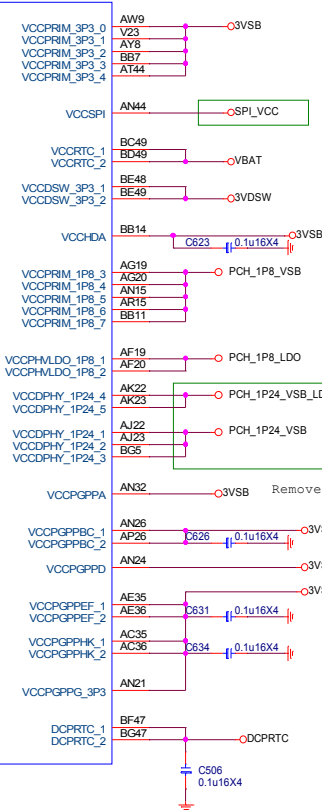






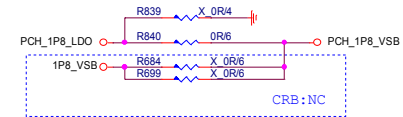


## POWER



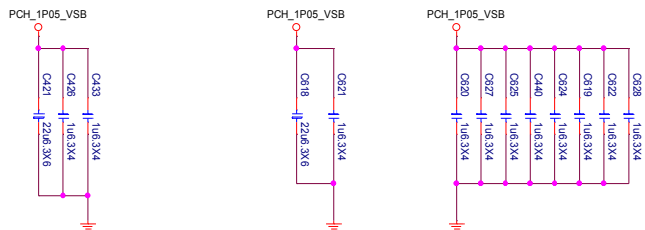
171213 Change to SPI\_VCC

PCH\_1P24\_VSB R1028 X 0R6 PCH\_1P24\_VSB\_LDO  
171212 Modify for Intel update  
with CNVI R1028 stuff  
no CNVI R1028 no stuff

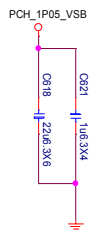


Remove GPPD Colay 1.8V

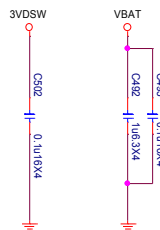
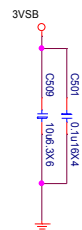
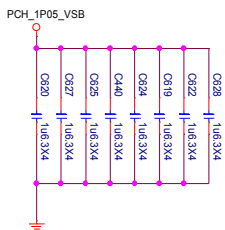
Remove GPPD Colay 1.8V



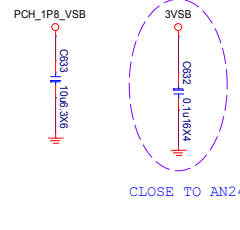
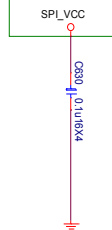
CLOSE TO B1/B2/B3/C1/C2



CLOSE TO U26/U29

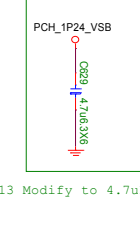


171213 Change to SPI\_VCC



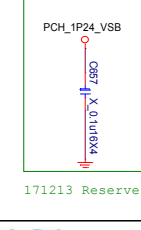
CLOSE TO AN24

Close to BG5

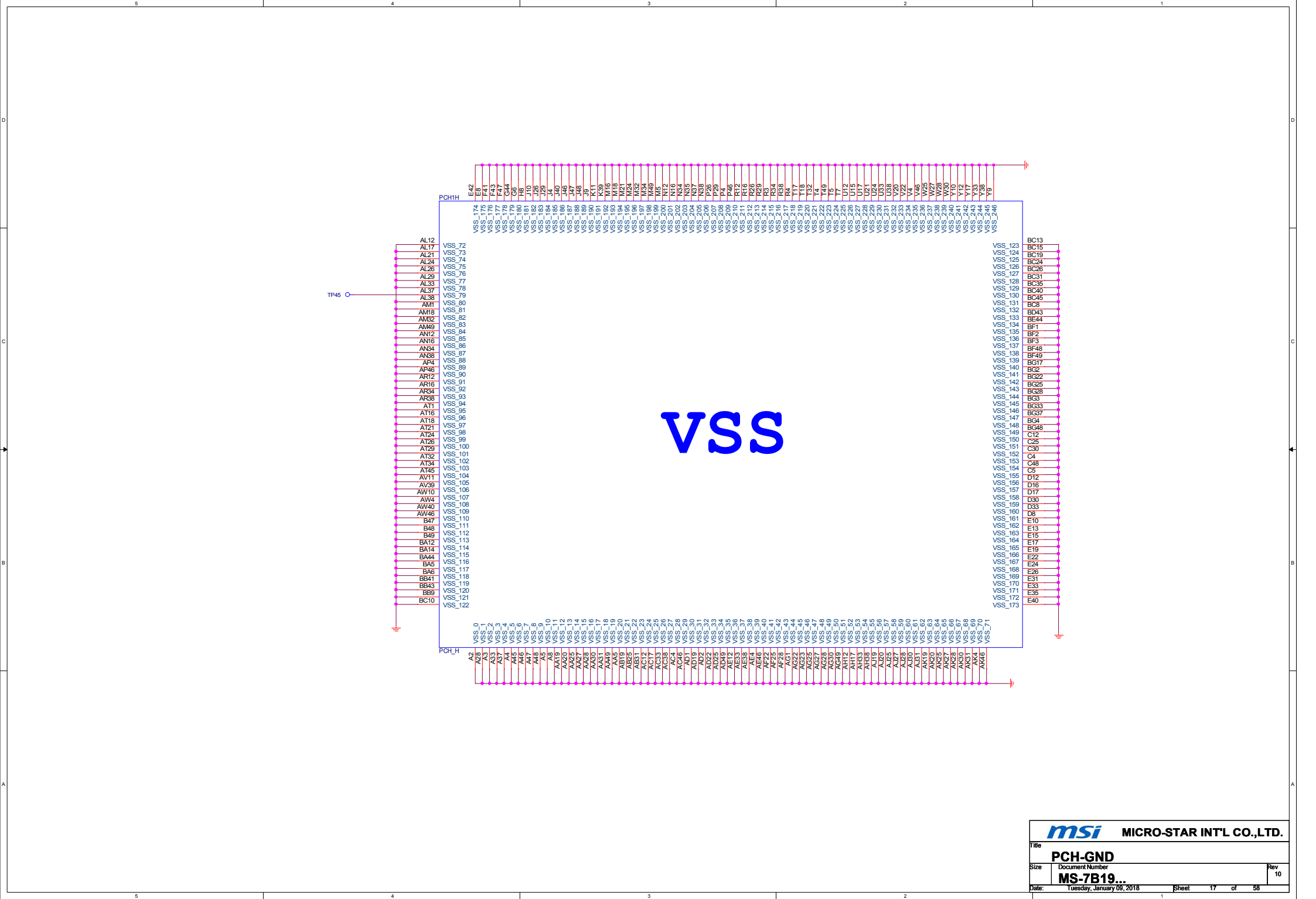


171213 Modify to 4.7uF(PDG)

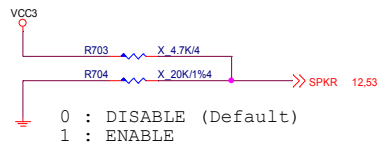
Close to AJ22, AJ23



171213 Reserve for AJ22, AJ23

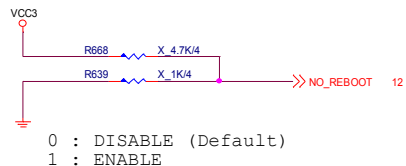


## TOP Swap



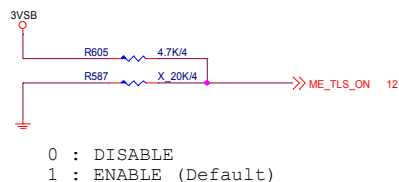
Internal pull-down is disabled after PCH\_PWROK is high.

## No Reboot



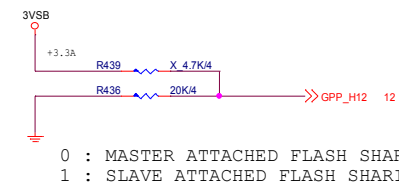
Internal pull-down is disabled after PCH\_PWROK is high.

## TLS confidentiality



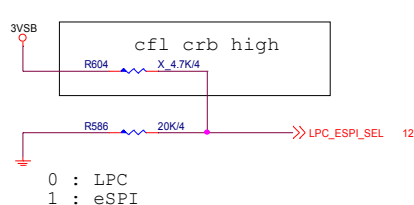
Internal pull-down is disabled after RSMRST# de-assert.

## ESPI FLASH SHARING MODE



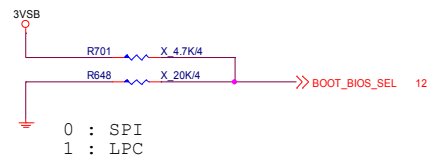
Internal pull-down is disabled after RSMRST# de-assert.

## LPC eSPI Mode



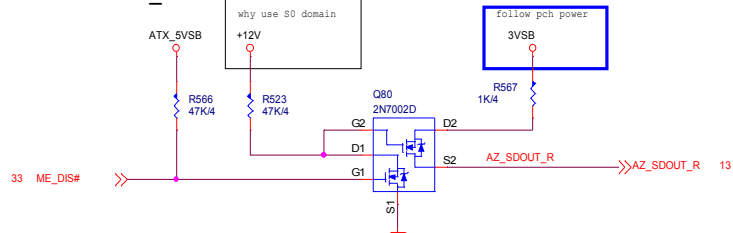
Internal pull-down is disabled after RSMRST# de-assert.

## Boot BIOS



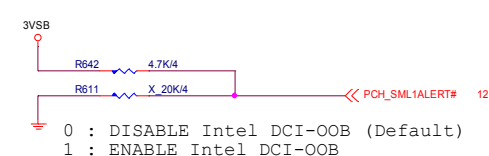
Internal pull-down is disabled after PCH\_PWROK is high.

## HDA\_SDO



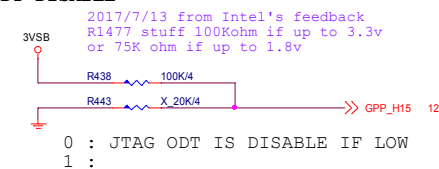
Internal pull-down is disabled after PCH\_PWROK is high.

## DCI ENABLE



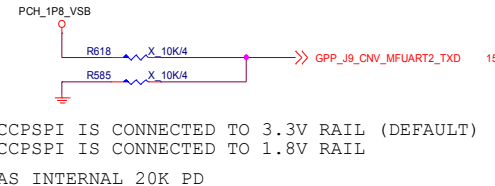
Internal pull-down is disabled after RSMRST# de-assert.

## ODT DISABLE



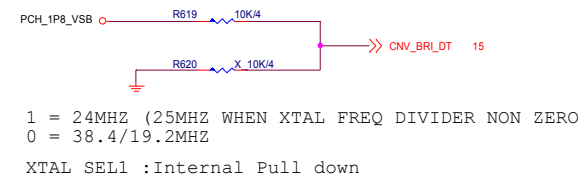
Internal pull-down is disabled after RSMRST# de-assert.

## SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE

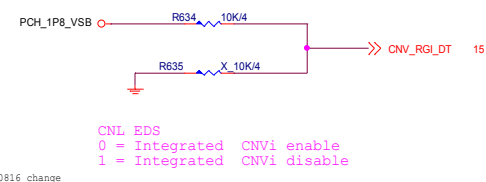


20170814 CHANGE

## XTAL FREQUENCY SELECTION

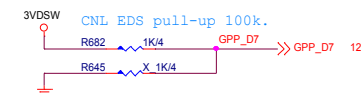


## MODEM AND NFC REFERENCE CLOCK SOURCE SELECT



20170816 change

## XTAL INPUT MODE



171213 Change to SPI\_VCC

Reserved  
SPL\_VCC  
2017/7/13 from Intel's feedback  
R1823 stuff 100Kohm if up to 3.3v  
or 75K ohm if up to 1.8v

20170814 CHANGE

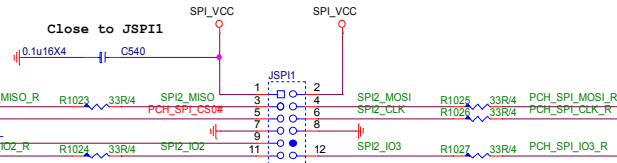
12 PCH\_SPI\_CS0# << PCH\_SPI\_CS0#  
 12,18 PCH\_SPI\_MOSI << PCH\_SPI\_MOSI R1018 0R/4 PCH\_SPI\_MOSI\_R  
 PCH\_SPI\_MISO << PCH\_SPI\_MISO R1019 0R/4 PCH\_SPI\_MISO\_R  
 12 PCH\_SPI\_CLK << PCH\_SPI\_CLK R1020 0R/4 PCH\_SPI\_CLK\_R  
 12,18 PCH\_SPI\_IO2 << PCH\_SPI\_IO2 R1021 0R/4 PCH\_SPI\_IO2\_R  
 12,18 PCH\_SPI\_IO3 << PCH\_SPI\_IO3 R1022 0R/4 PCH\_SPI\_IO3\_R

171212 Add for PDG,PDG->5ohm



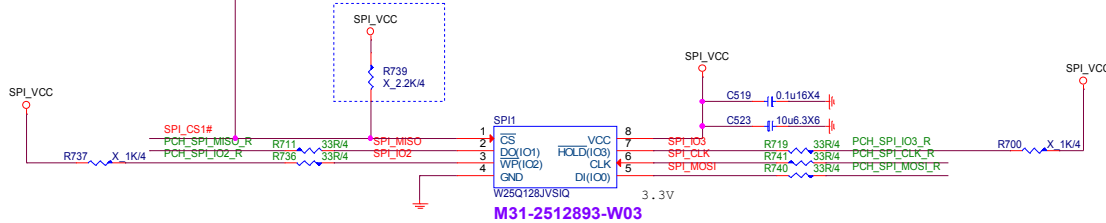
SPI CS# < 20pF  
 DOG-12A060C-A68

Close to JSP11

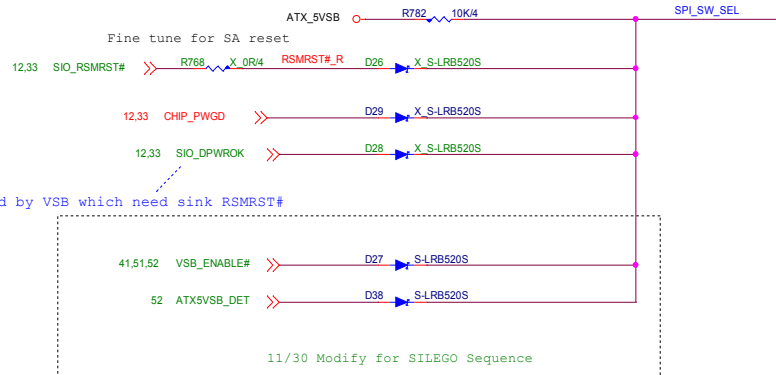


N31-2061451-H06

H2X8[10]M-2PITCH\_BLACK-RH-1



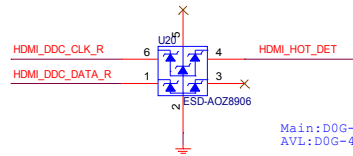
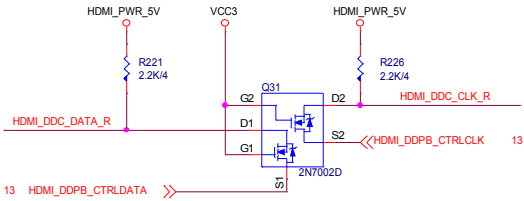
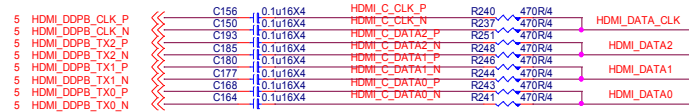
M31-2512893-W03



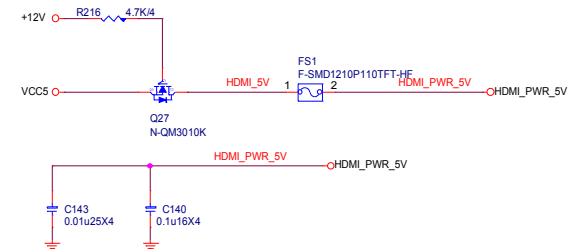
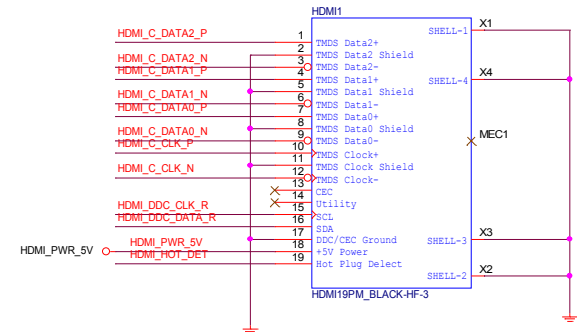
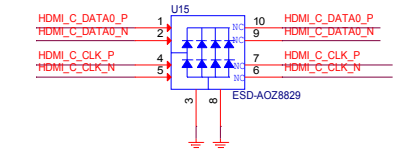
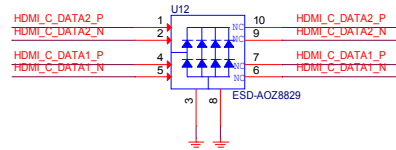
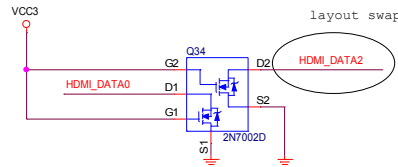
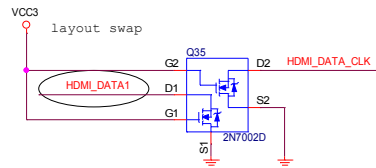
11/30 Modify for SILEGO Sequence

For TL624-1.1 (SKYLAKE)  
 In skylake, PCH core is powered by VSB which need sink RSMRST#  
 to low by SPI\_SW\_SEL.

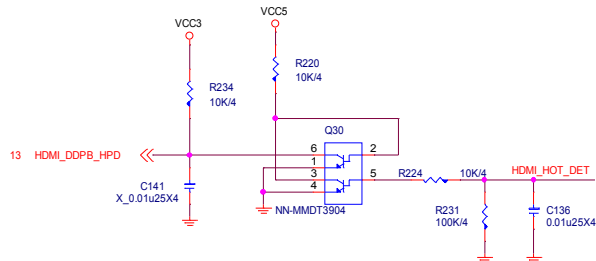
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



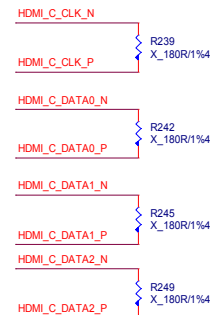
Main:D0G-05A0529-A68  
AVL:D0G-45B0510-II14



HPD



For EMI

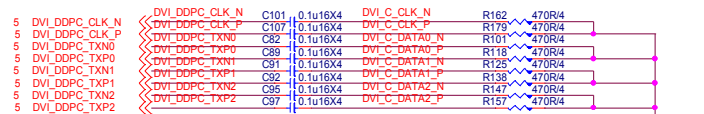


msi

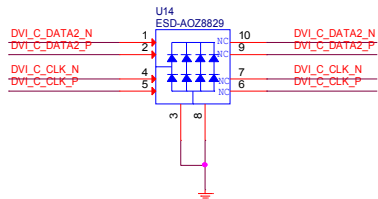
MICRO-STAR INT'L CO.,LTD.

Title			HDMI Connector
Size	Document Number	Rev	
	MS-7B19...	10	
Date:	Tuesday, January 09, 2018	Sheet	20 of 58

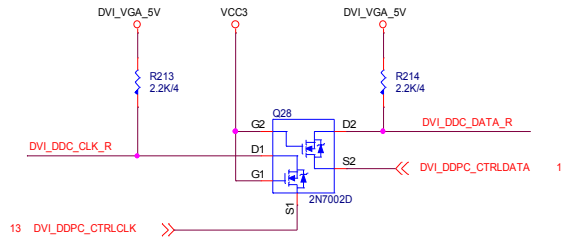
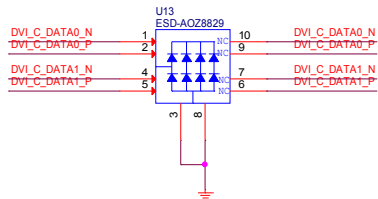
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



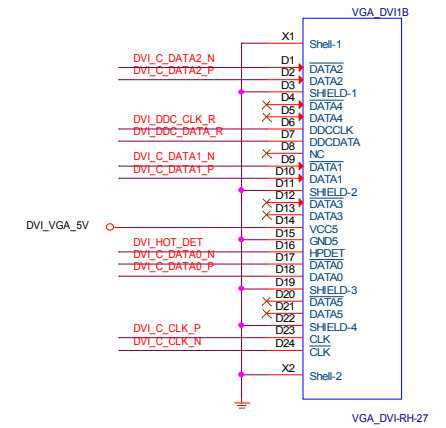
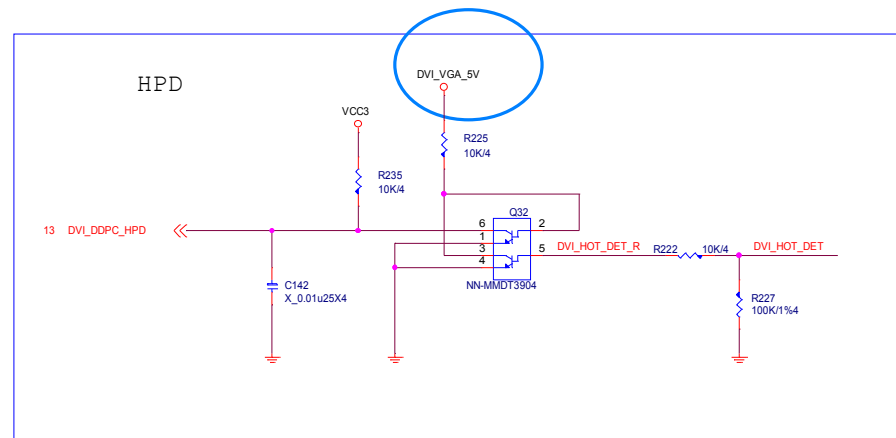
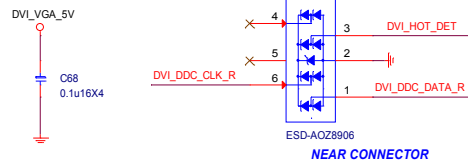
U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68



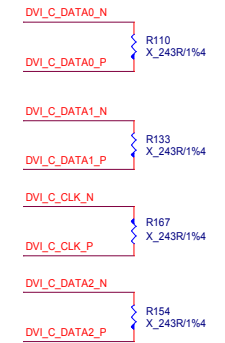
U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



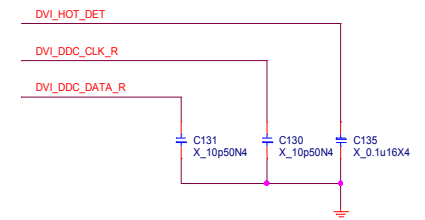
EMI Cap near connector DVI1



For EMI

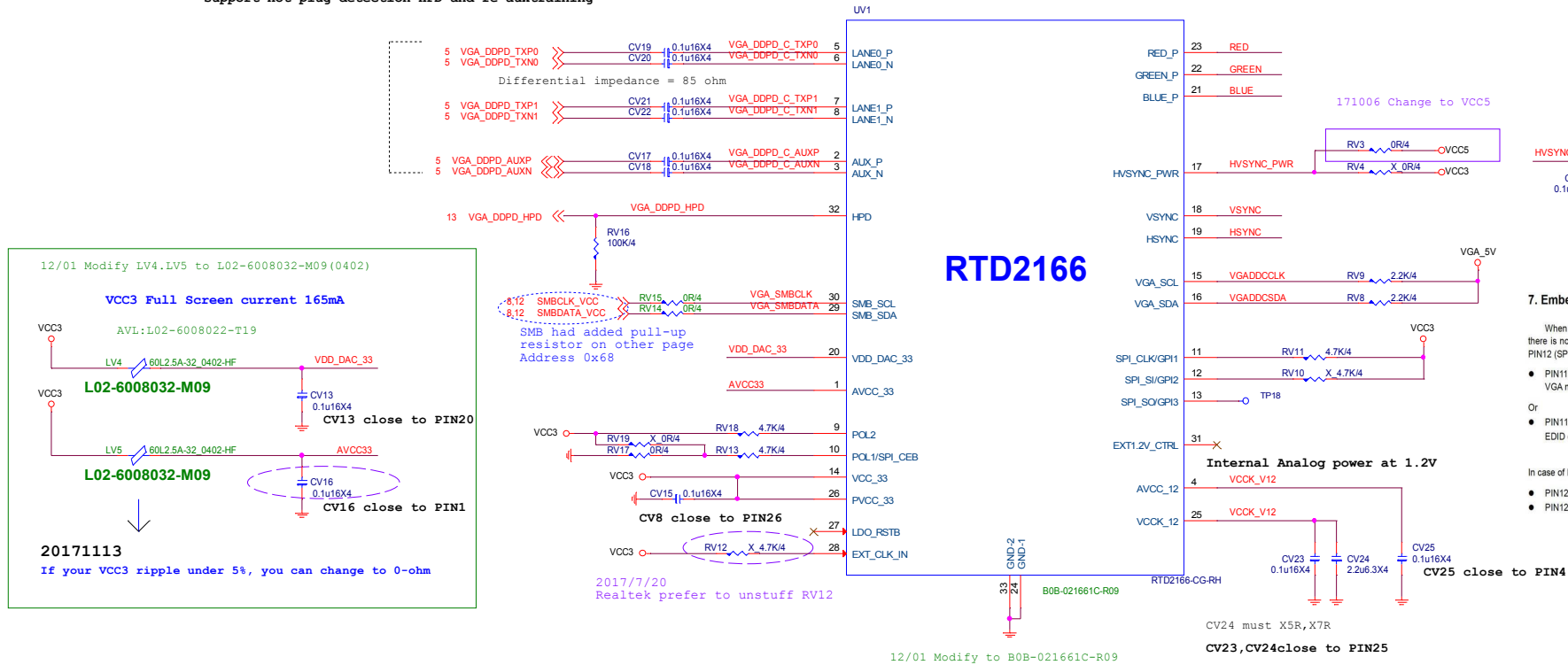


EMI



**Note:**

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

**7. Embedded EDID**

When operating RTD2166 in ROM mode, it could provide enable/disable EDID selection if there is no EDID on the VGA monitor. The configuration is defined by PIN11 (SPI\_CLK) and PIN12 (SPI\_SI) as follows.

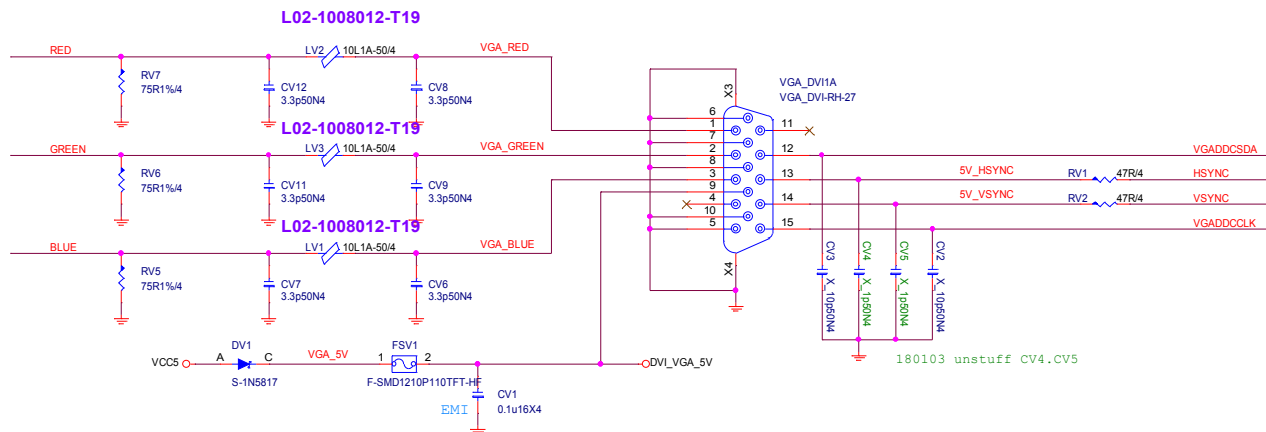
- PIN11 → 4.7KΩ Pull high, enable RTD2166 Embedded EDID if there is no EDID on the VGA monitor.

Or

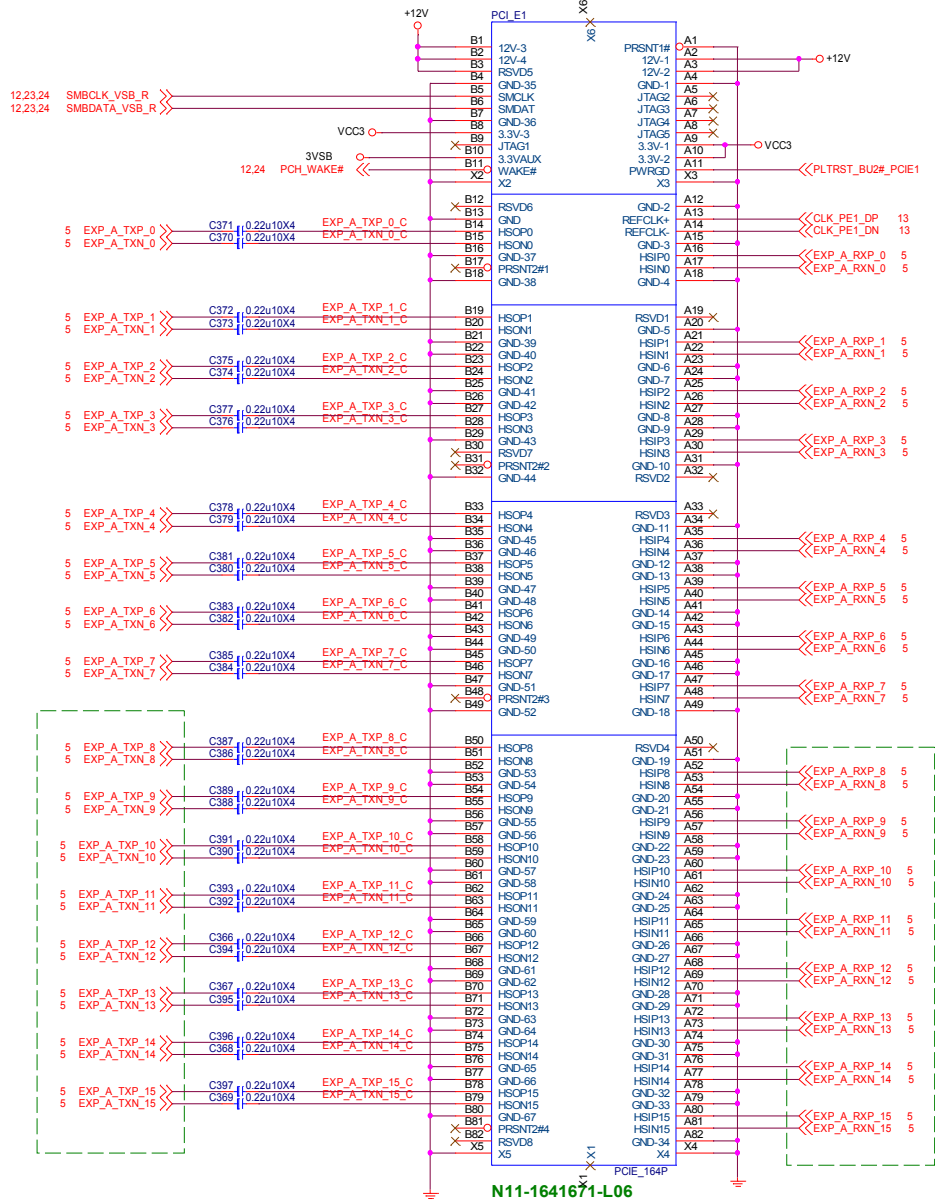
- PIN11 → 4.7KΩ Pull down (or N/C), disable RTD2166 Embedded EDID if there is no EDID on the VGA monitor. In this case, DP TX (CPU) will be in charge of the behavior.

In case of PIN11 Pull high with 4.7KΩ, PIN12 is use to choose RTD2166 Embedded EDID.

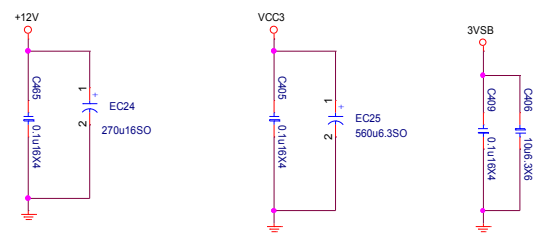
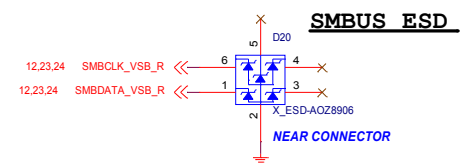
- PIN12 → 4.7KΩ Pull high, the maximum supported resolution is 1024x768
- PIN12 → 4.7KΩ Pull down (or N/C), the maximum supported resolution is 1920x1080





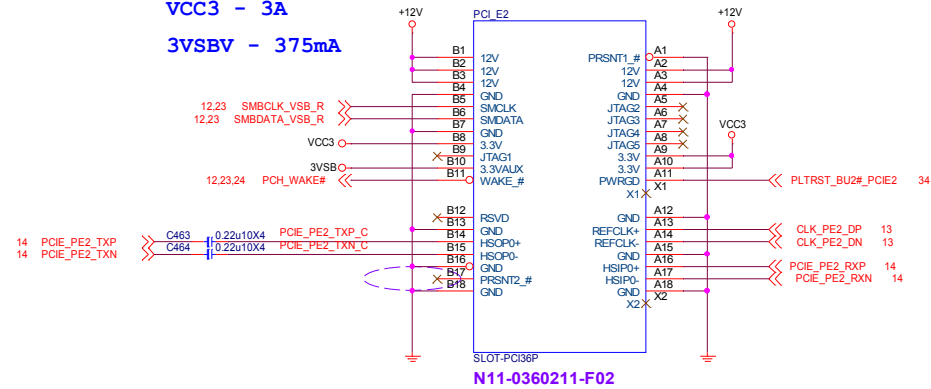


5.5A at +12V  
3A at VCC3  
375mA at 3VSB

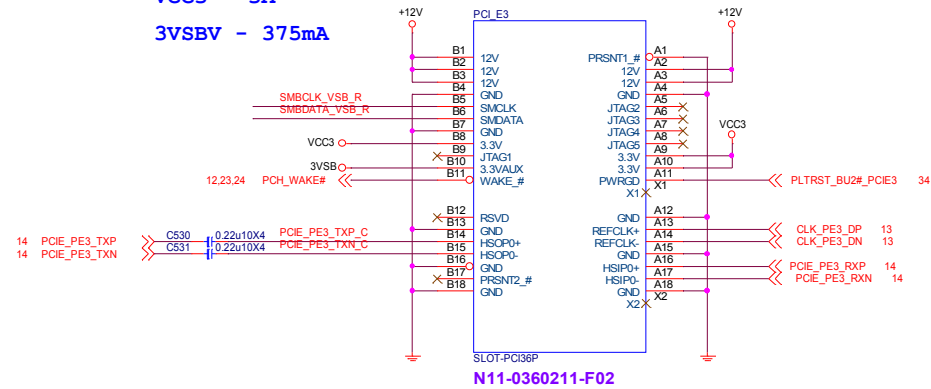


# PCH PCIE X1 Slot

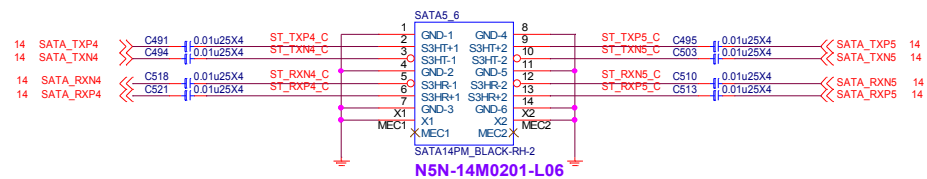
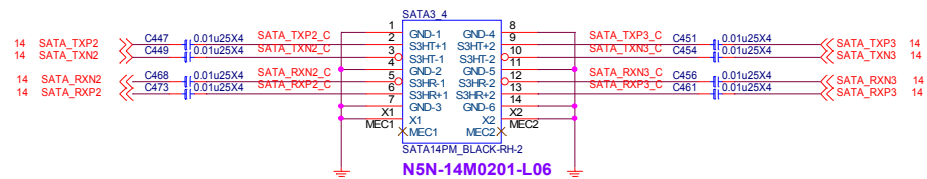
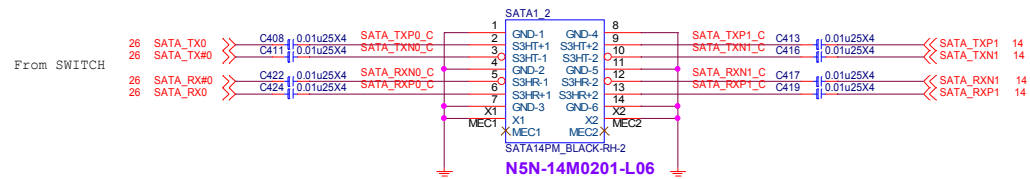
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



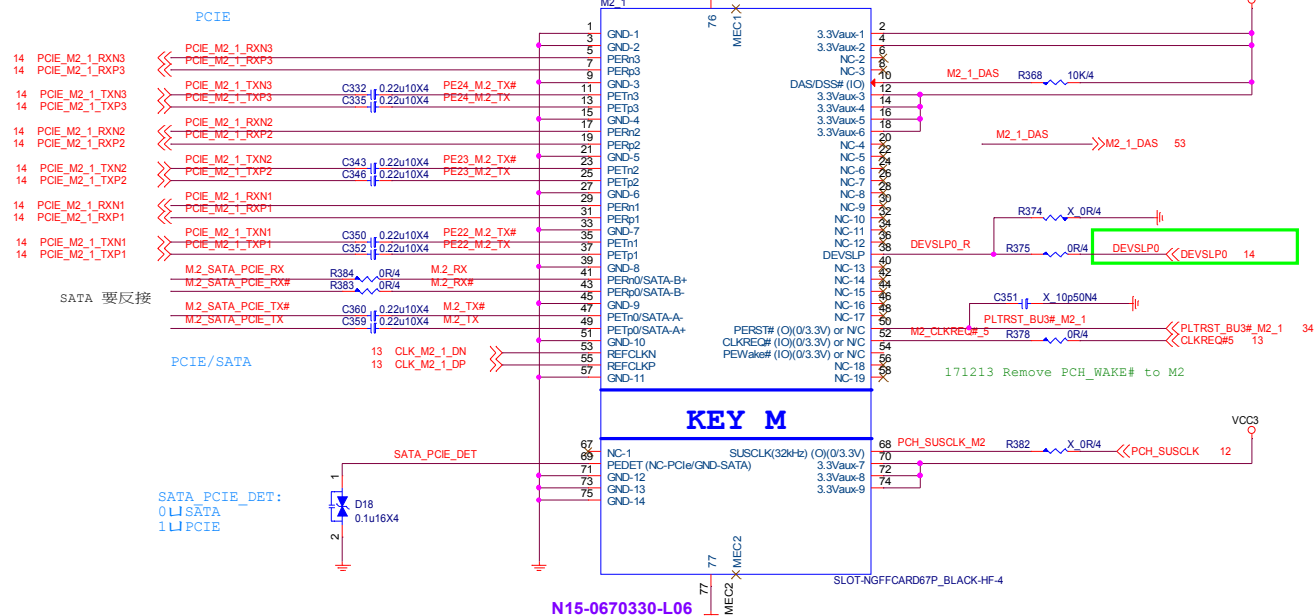
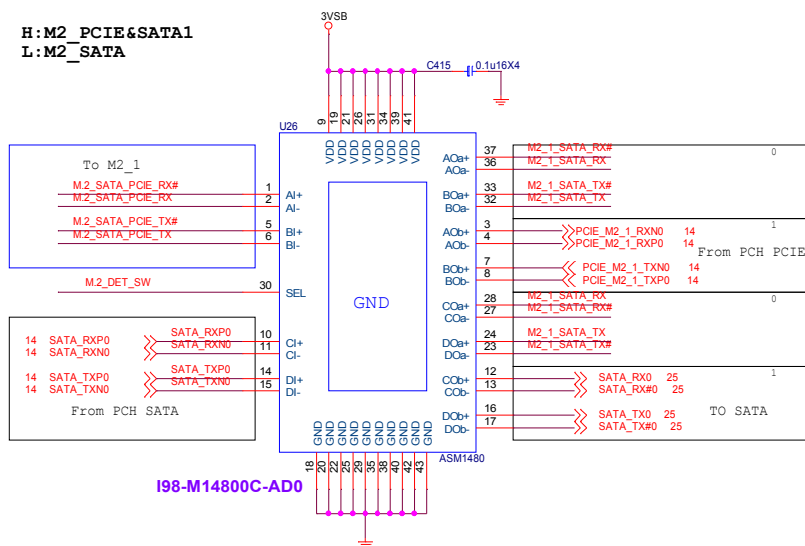
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



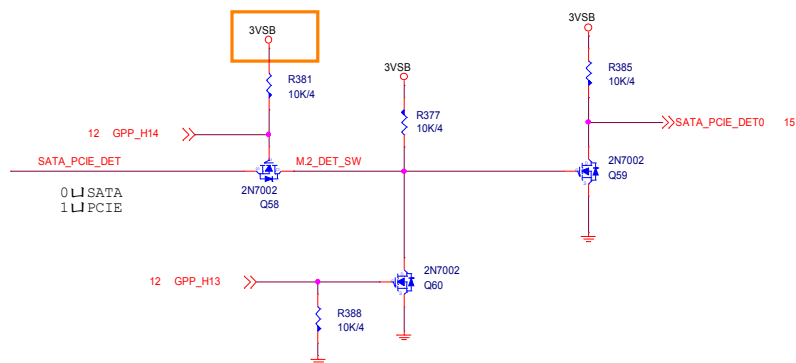
# **SATA 6G PORT 0.1**



```
H:M2_PCIE&SATA1
L:M2_SATA
```

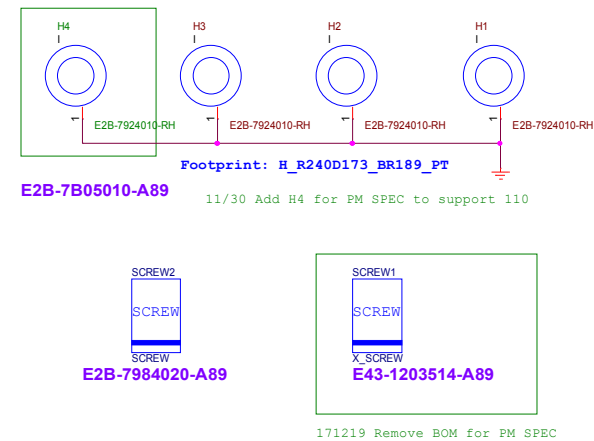
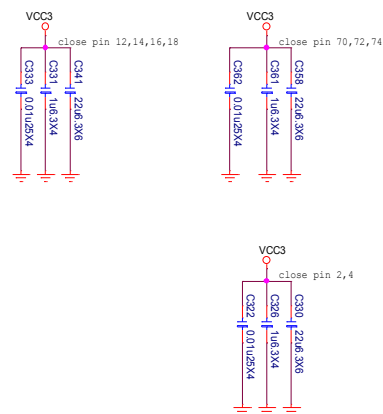


```
H:M2 SATA
L:M2-PCIE&SATA1
```

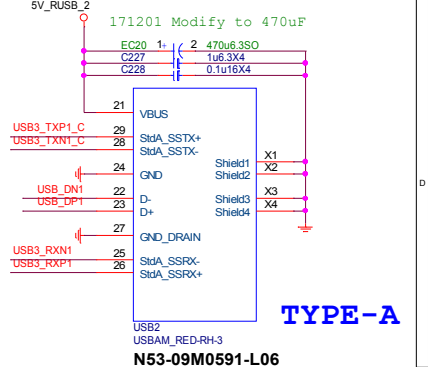
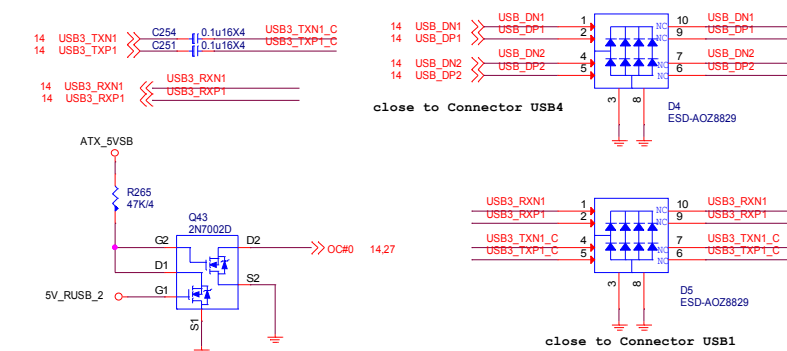
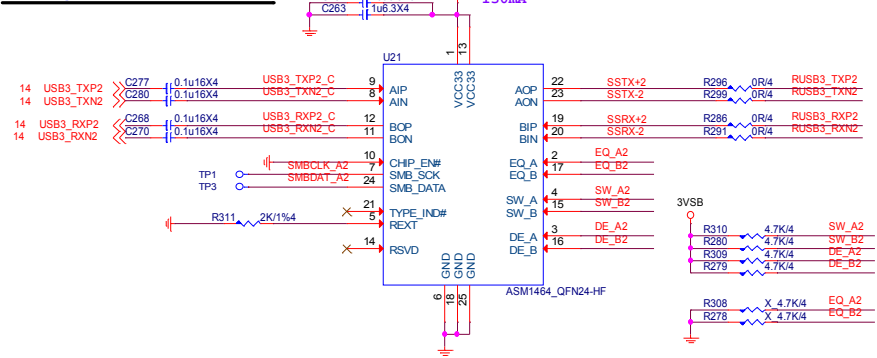


BIOS MODE

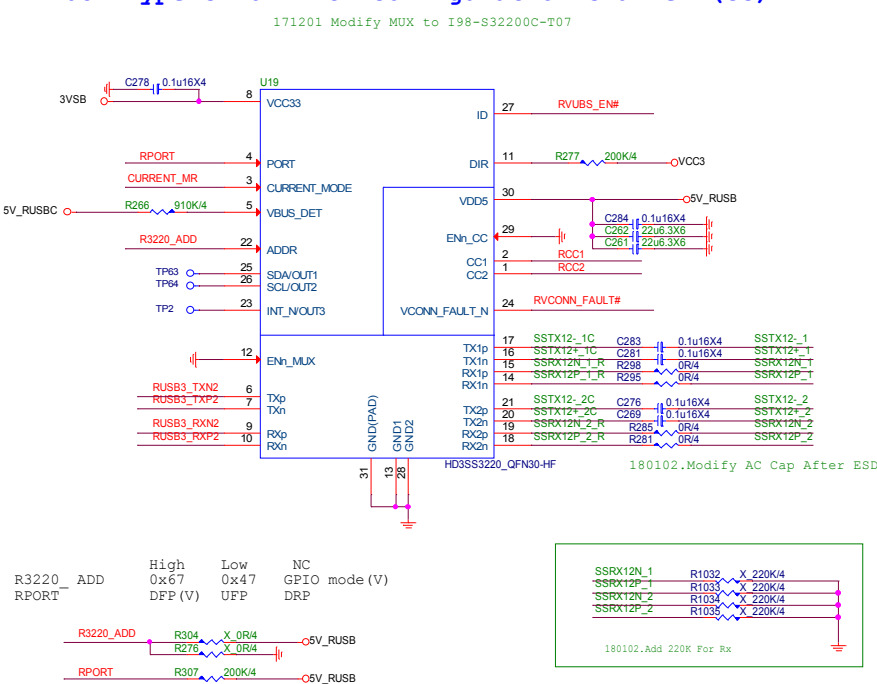
<i>GPP_H14</i>	<i>GPP_H13</i>	<i>Mode</i>		<i>GPP_K6</i>
0	1	M2-SATA	0	SATA1 M2_1_PCI-E
0	0	M2-PCI-E	1	M2_1_SATA
<i>GPI (1)</i>	<i>GPI (0)</i>	<i>AUTO</i>		



Rear Type C USB3.1 Redriver



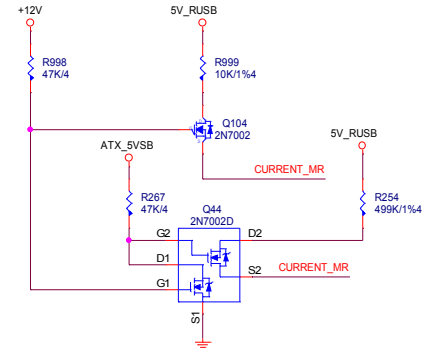
USB Type-C MUX with Configuration Channel (CC)



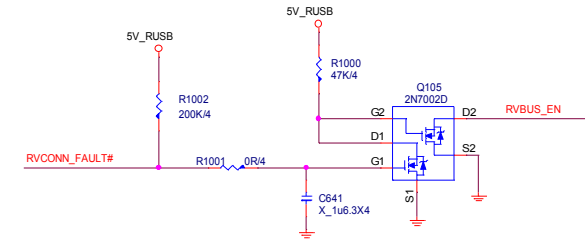
Current Mode

L - Default for 900mA  
M - Mid (500K) for 1.5A  
H - High (10K) for 3A

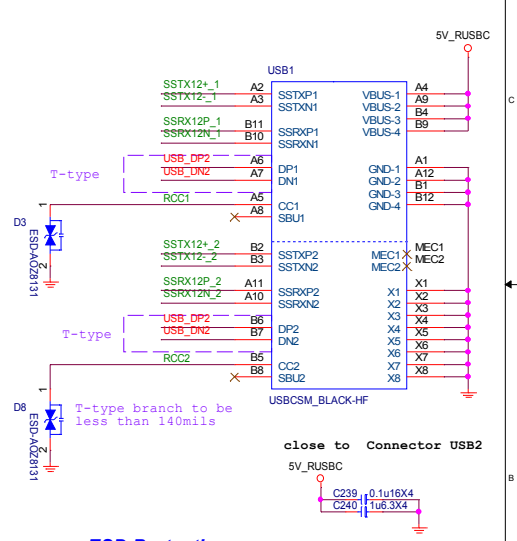
3A under S0 mode  
1.5A under S3 mode



VCONN OC#



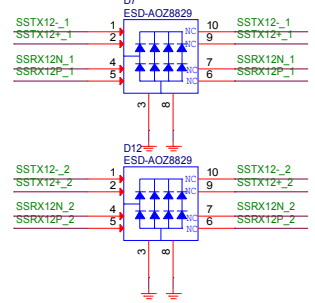
TYPE-C



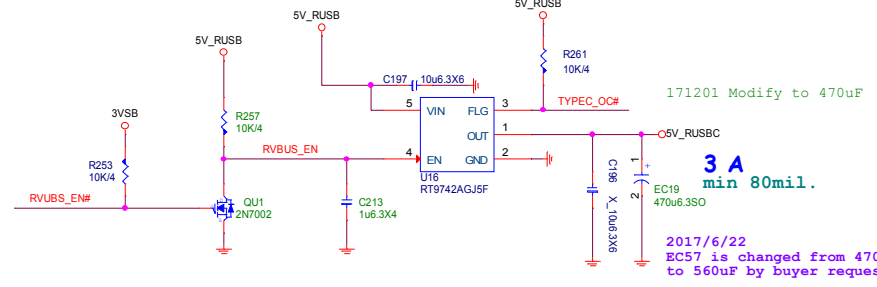
ESD Protection

180102.Modify AC Cap Before ESD

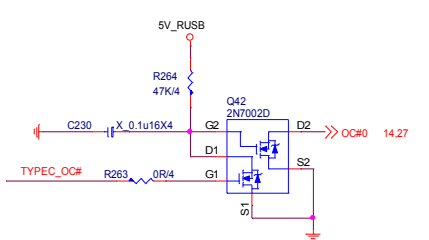
NEAR CONNECTOR



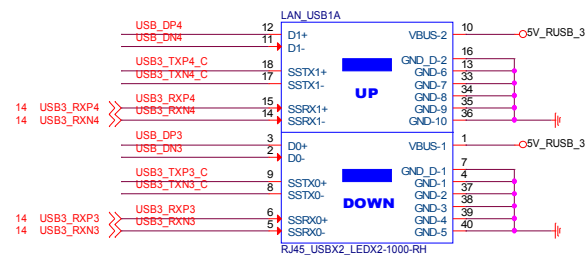
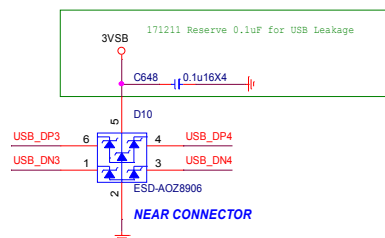
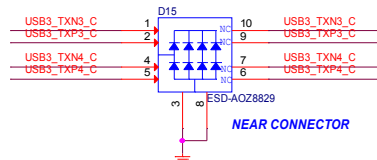
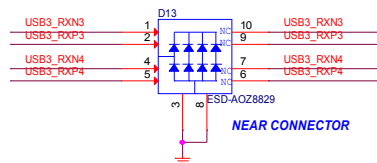
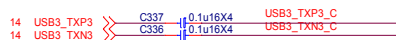
VBUS



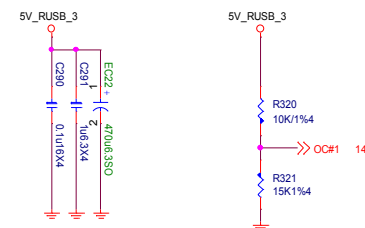
VBUS OC#



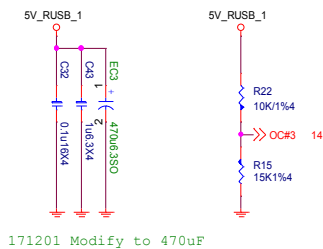
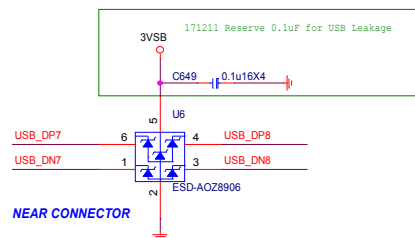
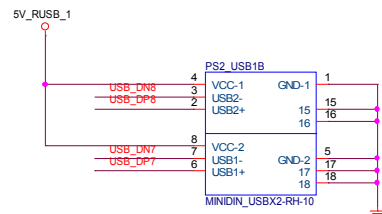
## LAN USB1



171201 Modify to 470uF

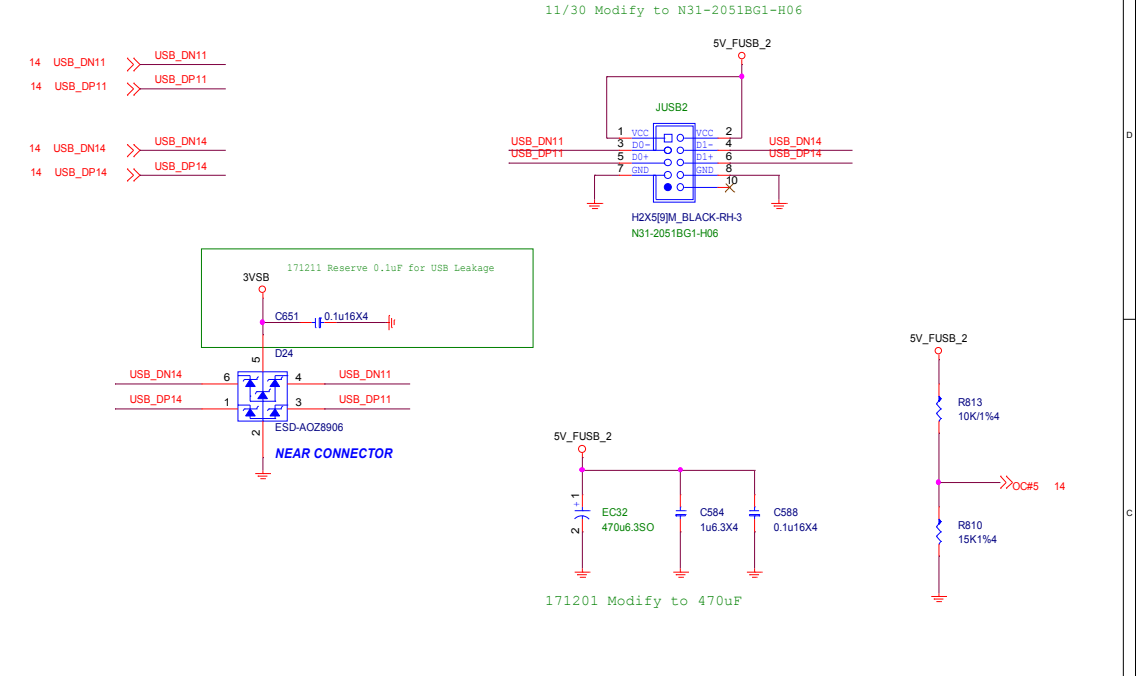
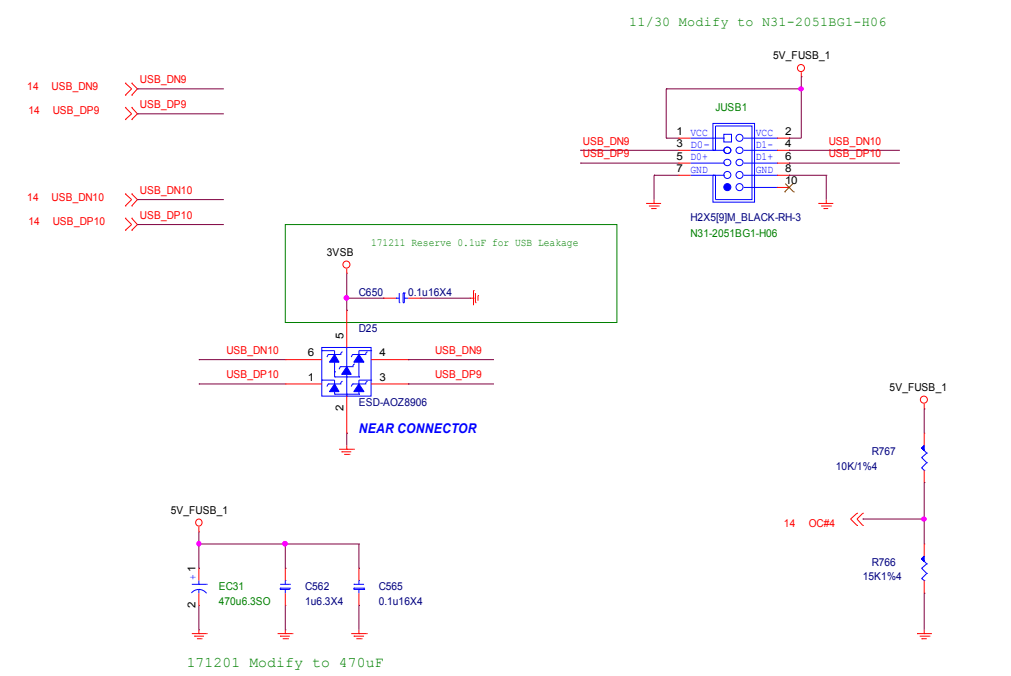


## PS2\_USB1

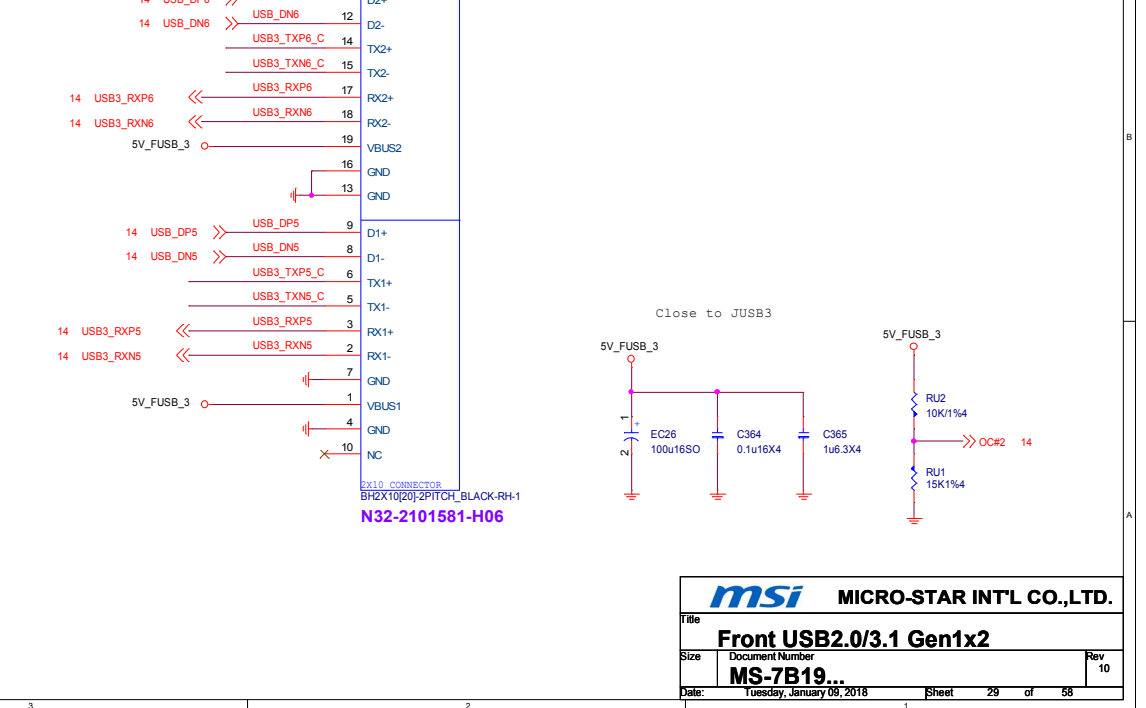
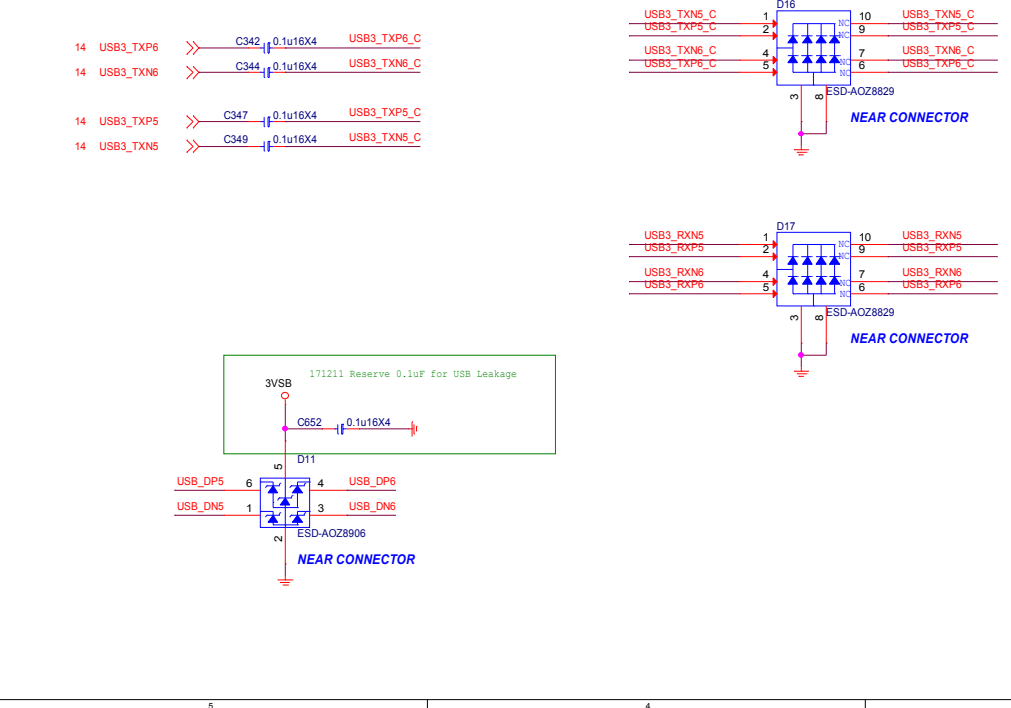


171201 Modify to 470uF

FRONT USB2.0



FRONT USB3.0  
180

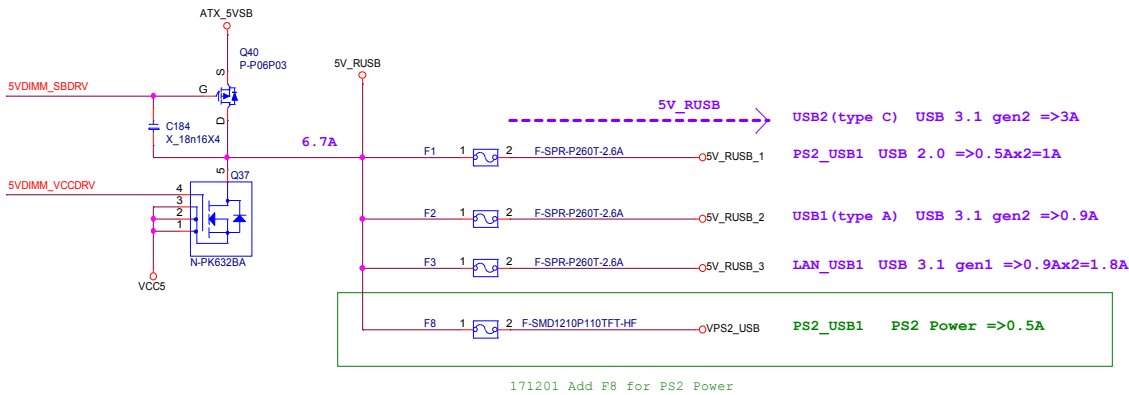




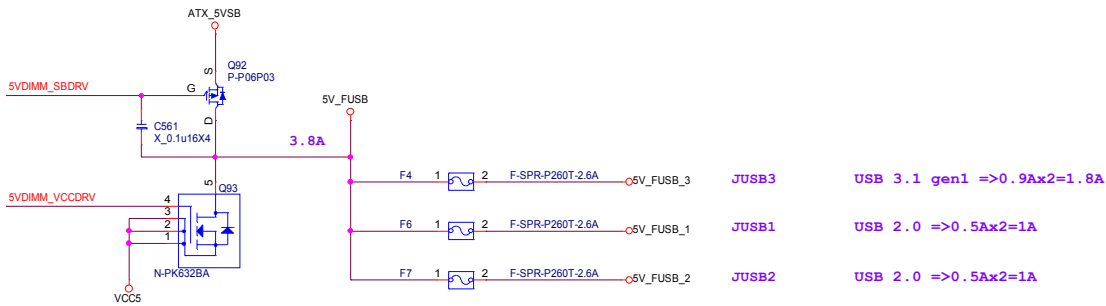
USB POWER

41 5VDIMM\_SBDRV << 5VDIMM\_SBDRV  
41 5VDIMM\_VCCDRV << 5VDIMM\_VCCDRV

REAR USB PORT POWER

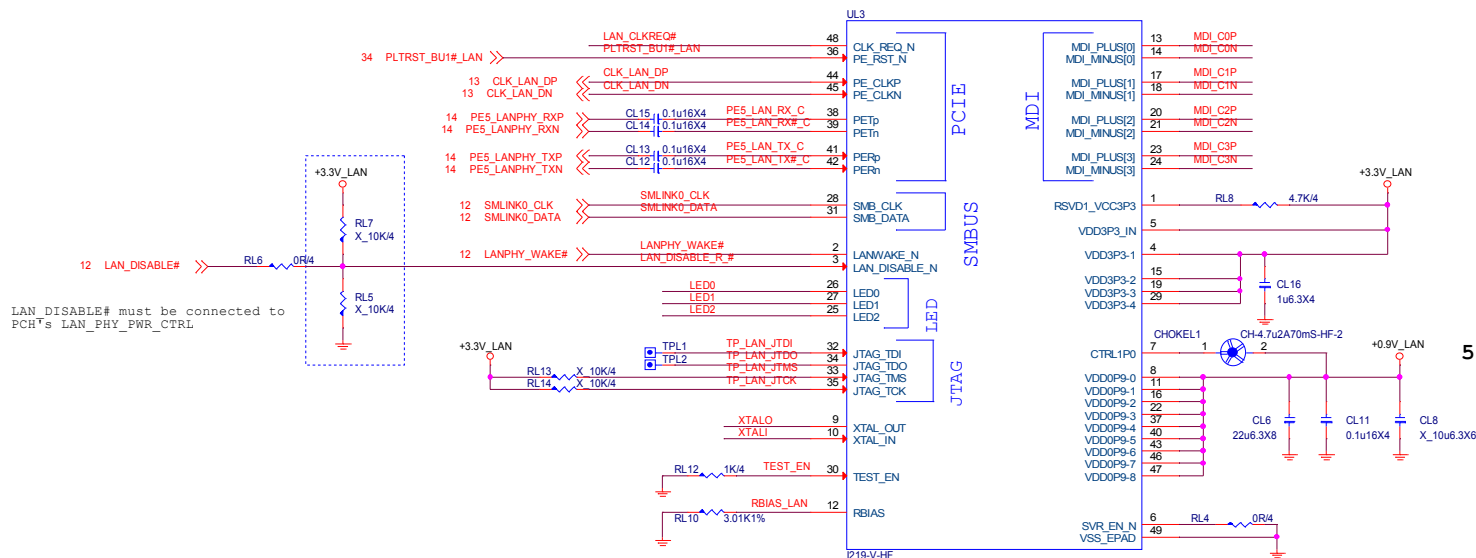


FRONT USB PORT POWER

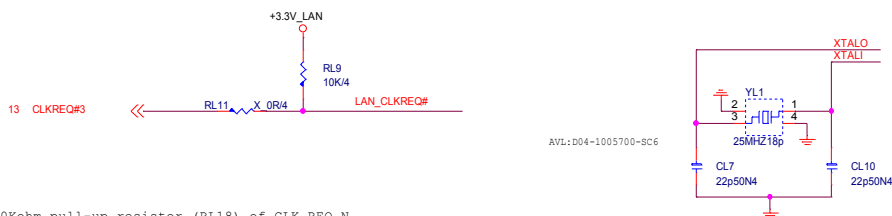


Intel Lan- i219

8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

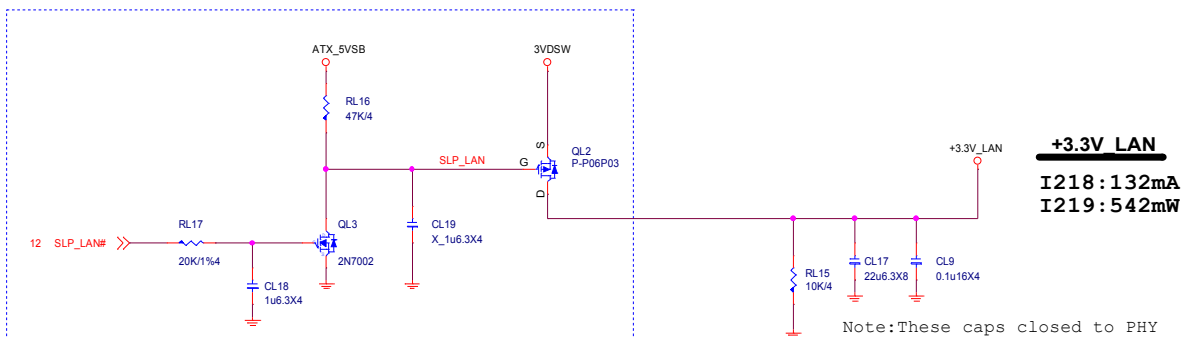


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.  
If CLK REQ N is not used, pin48 is pulled up 10K $\Omega$  to 3.3V LAN



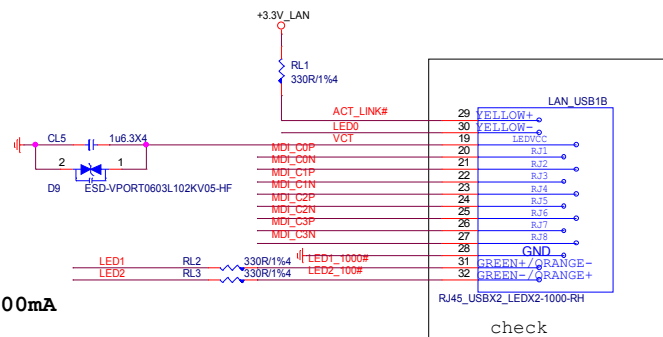
The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

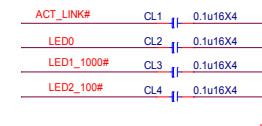


Note: These caps closed to PHY

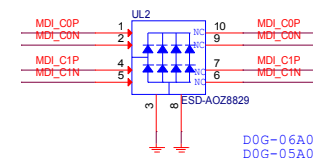
## LAN Connector



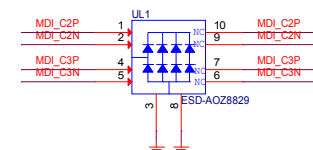
*For EMI*



UL2&UL3 close to connector

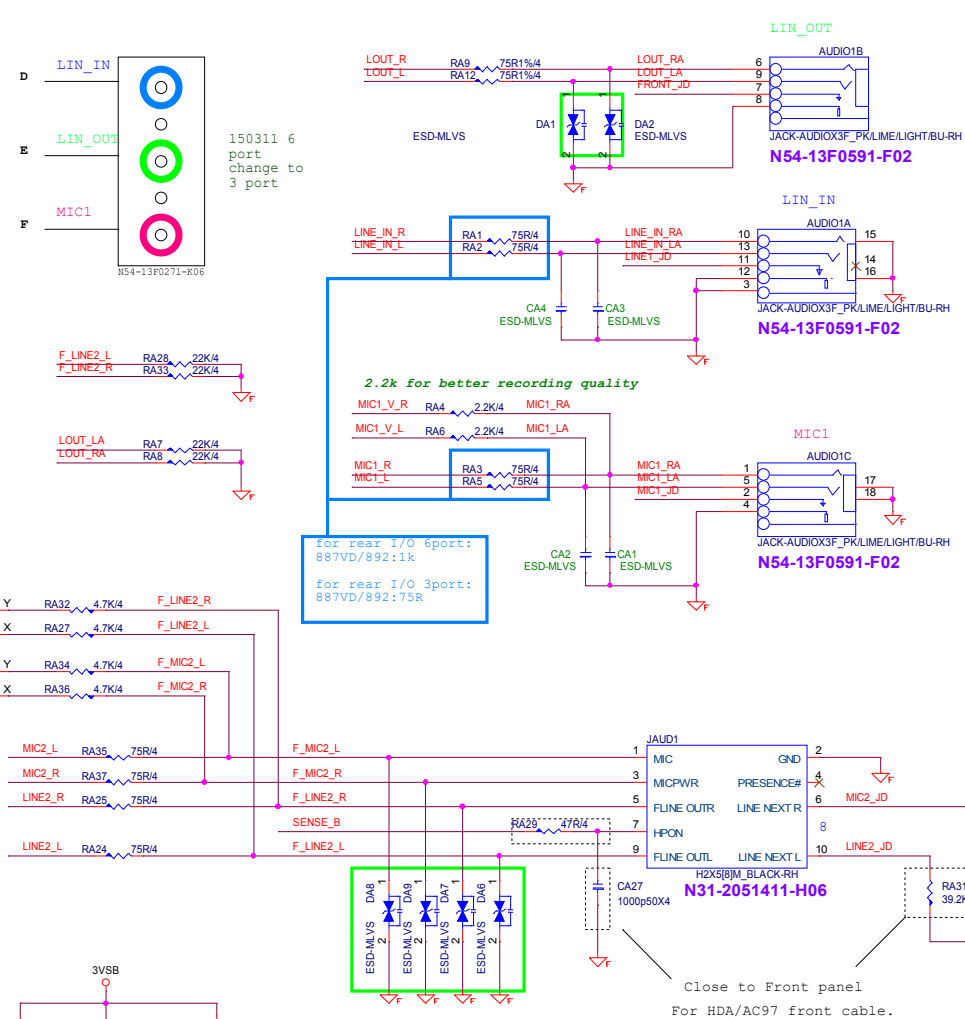
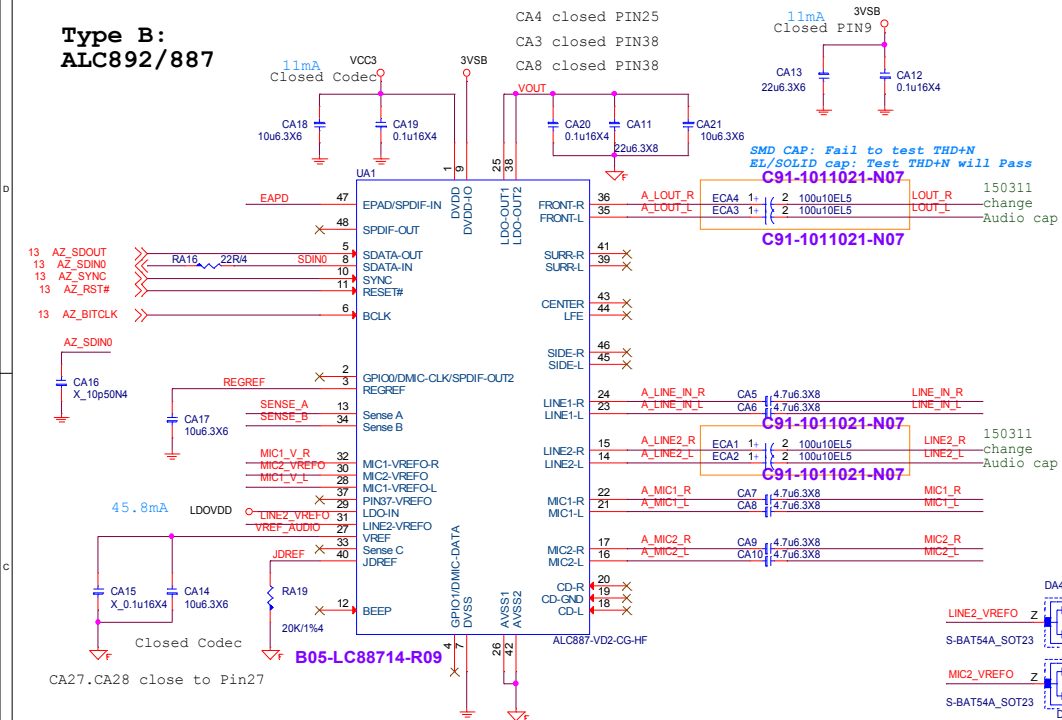


D0G-06A050C-A68  
D0G-05A0300-I14



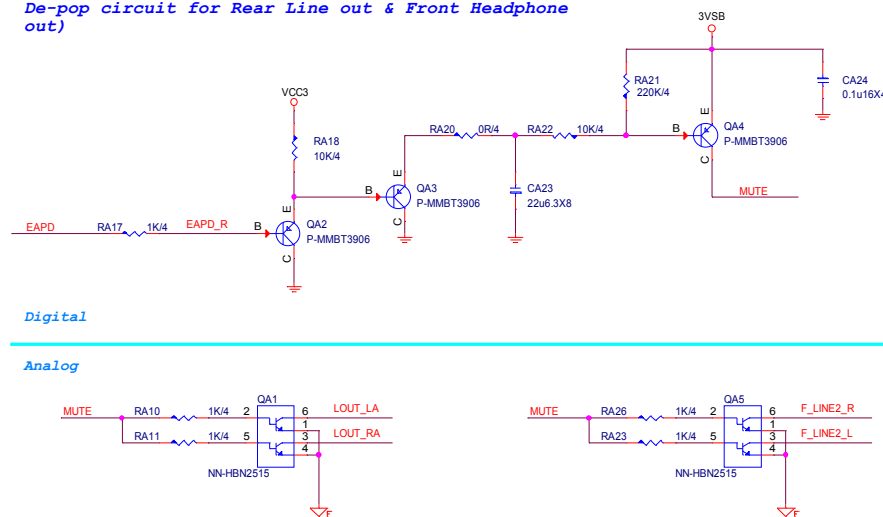
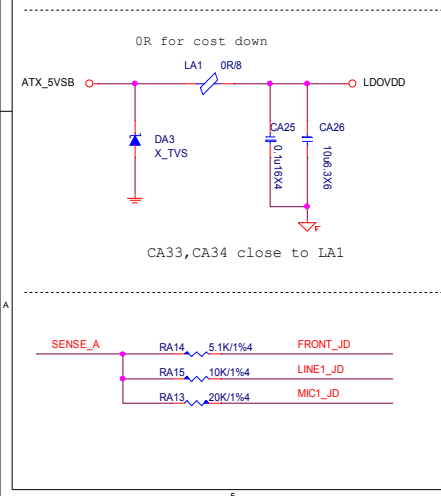
Do not pair MDI0 and MDI1 on the same TVSdevice  
(avoid LAN POE connecting issue).  
Otherpairing combination is ok.

Type B:  
ALC892/887

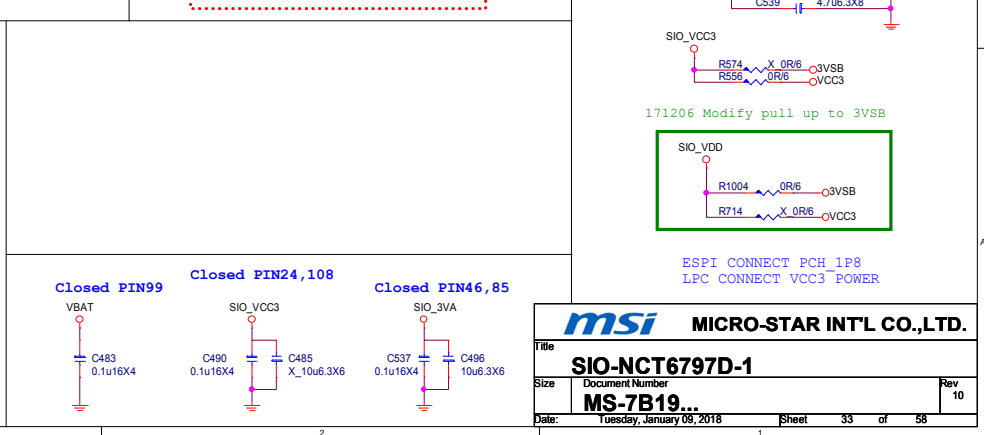
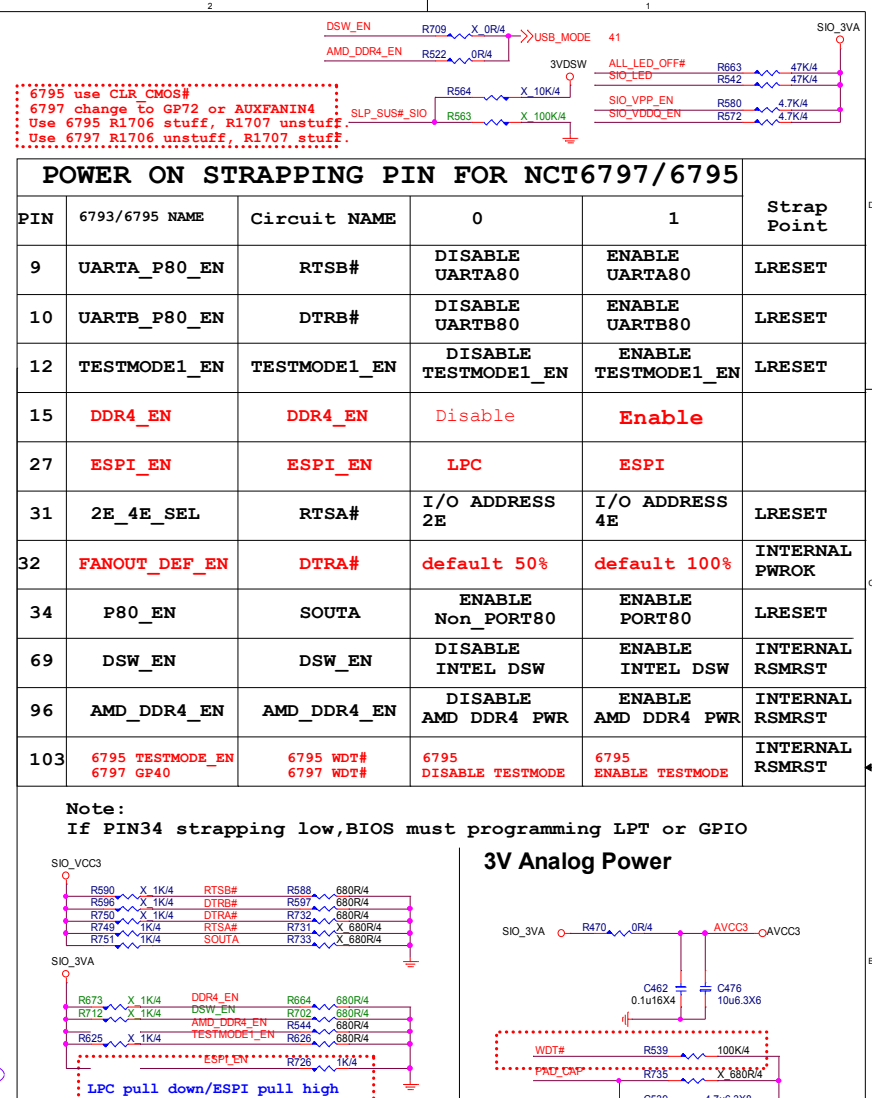


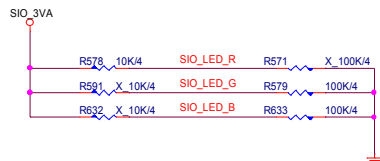
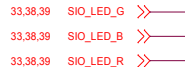
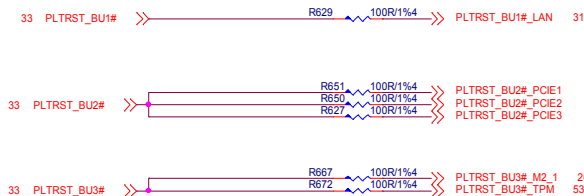
### Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Varister --> cap for cost down  
D0G-2950500-SI0  
D0G-3010510-I05  
Close to Jack

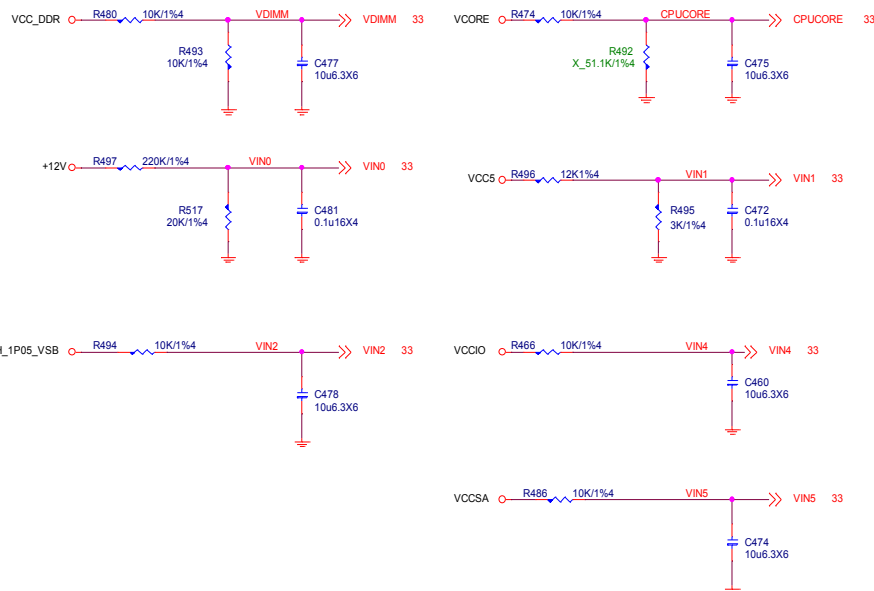




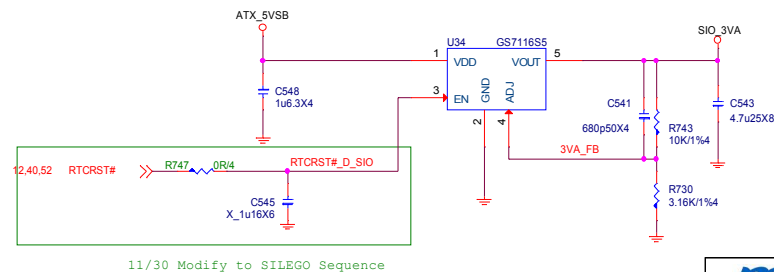
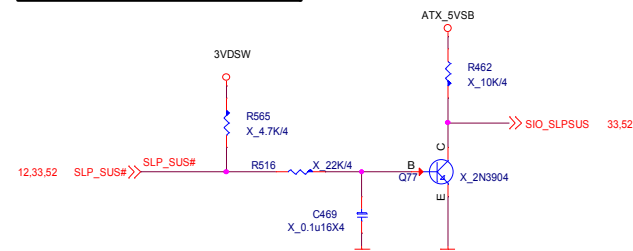
11/30 Remove PCH\_1P05\_VSB to RSMRST# Circuit

## HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



## SLP\_SUS Co-lay circuit



# SERIAL PORT 1

The schematic diagram illustrates the SERIAL PORT 1 circuit. It includes a power supply section with SIO\_VCC3 and a +12V COM supply. The main component is a microcontroller (U33) with pins VDD, VSS, and various signal pins (RA1, RA2, RA3, RA4, RA5, DA1, DA2, DA3, GND). The circuit also features a 1N4148W diode (D35) and a 0.1u16X4 capacitor (C560). The output section includes a 1N4148W diode (D23) and a 0.1u16X4 capacitor (C542). The circuit is labeled with various component values and pin numbers.

**NO USE UART PORT1**

**N31-2051331-H06**

**Component List:**

- R752: X 2.7K/4 SINA
- R757: X 2.7K/4 CTSA#
- R763: X 2.7K/4 RIA#
- R748: X 2.7K/4 DCCA#
- R756: X 2.7K/4 DSRSA#
- NDCDA#: 1 JCOM1 2 NSINA
- NSOUTA: 3 4 NDTRA
- 5 6 NDSRA#
- NRTSA: 7 8 NCTSA#
- NRIA: 9
- H2X5[10]M\_BLACK-RH
- C551: X 0.1u16X4
- C560: 0.1u16X4
- C556: X 470p50X4
- C557: X 470p50X4
- C558: X 470p50X4
- C559: X 470p50X4
- C552: X 470p50X4
- C553: X 470p50X4
- C554: X 470p50X4
- C555: X 470p50X4

**Pin Connections:**

- VCC5: 20 VCC
- NRIA: 2
- NCTSA#: 3
- NDSRA#: 4
- NSINA: 7
- NDCDA#: 9
- RTSA#: 16
- DTRA#: 15
- SOUTA: 13
- DA1: 11
- DA2: 15
- DA3: 13
- GND: 11
- VDD: 1
- RY1: 18
- RY2: 17
- RY3: 14
- RY4: 12
- RY5: 10
- DA1: 5
- DA2: 6
- DA3: 8
- GND: 10
- VSS: 10
- RIA#: 33
- CTSA#: 33
- DSRA#: 33
- SINA: 33
- DCCA#: 33
- NRTSA: 33
- NDTRA: 33
- NSOUTA: 33
- 12V\_COM: 33
- 12V\_LCOM: 33

**PARALLEL PORT**

VCC5  $\rightarrow$  D37 1N4148W A C LPT\_VC

C586  $\parallel$  0.1u16X4

33 PPRND3  $\gg$  PPRND3 R776  $\gg$  33R/4 PRND3 R798  $\gg$  2.7K/4

33 PPRND2  $\gg$  PPRND2 R775  $\gg$  33R/4 PRND2 R797  $\gg$  2.7K/4

33 PPRND1  $\gg$  PPRND1 R772  $\gg$  33R/4 PRND1 R794  $\gg$  2.7K/4

33 PPRND0  $\gg$  PPRND0 R771  $\gg$  33R/4 PRND0 R792  $\gg$  2.7K/4

33 PPRND4  $\gg$  PPRND4 R777  $\gg$  33R/4 PRND4 R799  $\gg$  2.7K/4

33 PPRND5  $\gg$  PPRND5 R778  $\gg$  33R/4 PRND5 R800  $\gg$  2.7K/4

33 PPRND6  $\gg$  PPRND6 R779  $\gg$  33R/4 PRND6 R801  $\gg$  2.7K/4

33 PPRND7  $\gg$  PPRND7 R780  $\gg$  33R/4 PRND7 R802  $\gg$  2.7K/4

33 STB#  $\gg$  STB# R789  $\gg$  33R/4 RSTB# R790  $\gg$  2.7K/4

33 SLIN#  $\gg$  SLIN# R774  $\gg$  33R/4 RSLIN# R796  $\gg$  2.7K/4

33 INIT#  $\gg$  INIT# R773  $\gg$  33R/4 RINIT# R795  $\gg$  2.7K/4

33 AFD#  $\gg$  AFD# R770  $\gg$  33R/4 RAFFD# R791  $\gg$  2.7K/4

33 RACK#  $\gg$  RACK# R785  $\gg$  2.7K/4

33 RBUSY  $\gg$  RBUSY R786  $\gg$  2.7K/4

33 RPE  $\gg$  RPE R787  $\gg$  2.7K/4

33 RSLCT  $\gg$  RSLCT R788  $\gg$  2.7K/4

33 RERR#  $\gg$  RERR# R793  $\gg$  2.7K/4

PRND0 C568  $\times$  470p50X4

PRND1 C570  $\times$  470p50X4

PRND2 C573  $\times$  470p50X4

PRND3 C574  $\times$  470p50X4

PRND7 C578  $\times$  470p50X4

PRND6 C577  $\times$  470p50X4

PRND5 C576  $\times$  470p50X4

PRND4 C575  $\times$  470p50X4

RSTB# C566  $\times$  470p50X4

RSLIN# C572  $\times$  470p50X4

RINIT# C571  $\times$  470p50X4

RAFFD# C567  $\times$  470p50X4

RACK# C579  $\times$  470p50X4

RBUSY C580  $\times$  470p50X4

RPE C581  $\times$  470p50X4

RSLCT C582  $\times$  470p50X4

RERR# C569  $\times$  470p50X4

JLPT1

H2X13J26M\_BLACK-RH

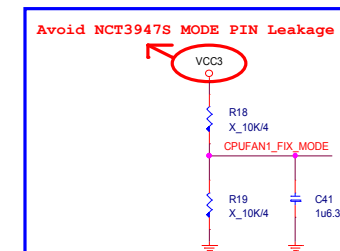
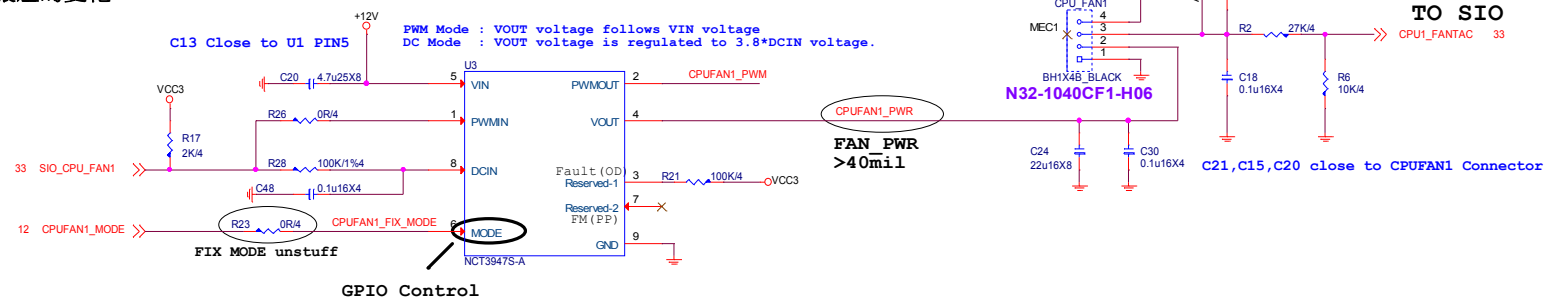
**N31-2131131-H06**

**N31-2131151-H06 : 2.0mm**

**N31-2131131-H06 : 2.54mm**

```
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
```

1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCF拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化



Resever For FIX DC or PWM MODE USE By PM SPEC

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

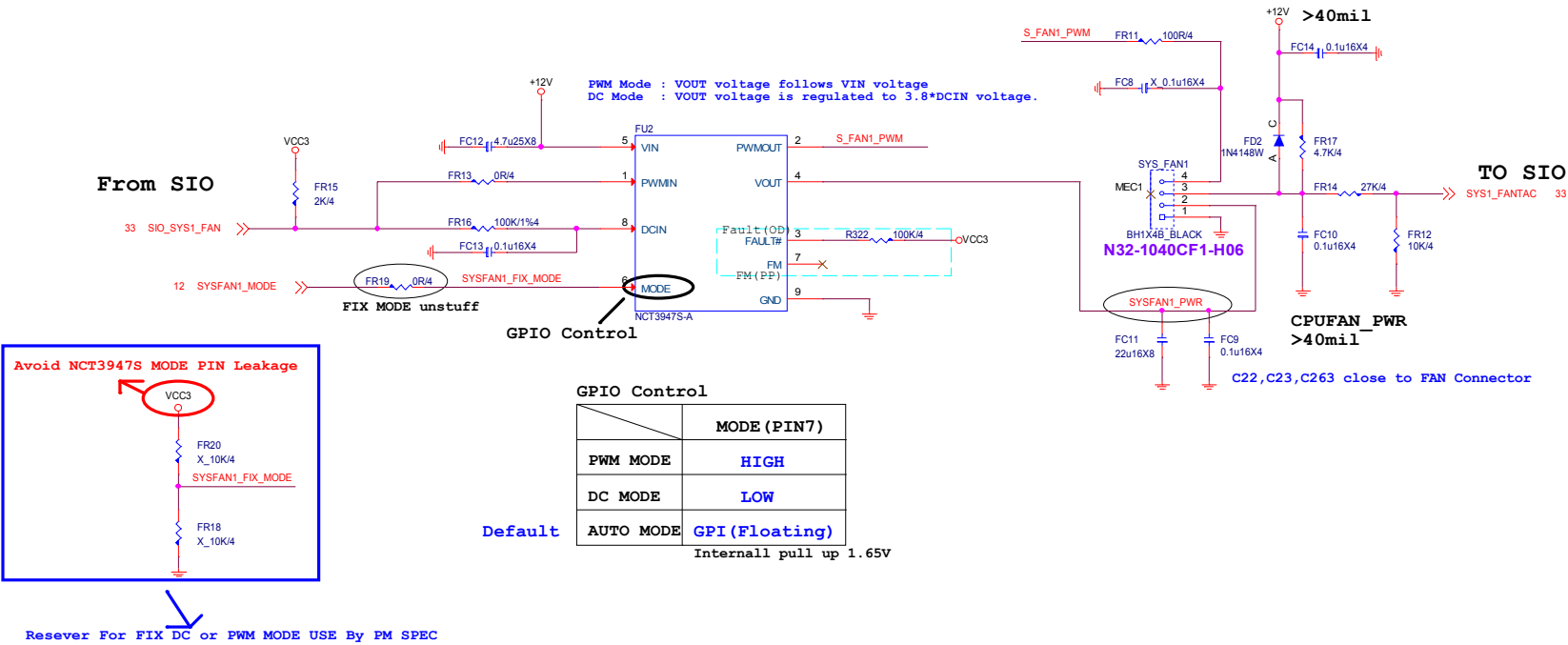
### Default

Internall pull up 1.65V	
-------------------------	--

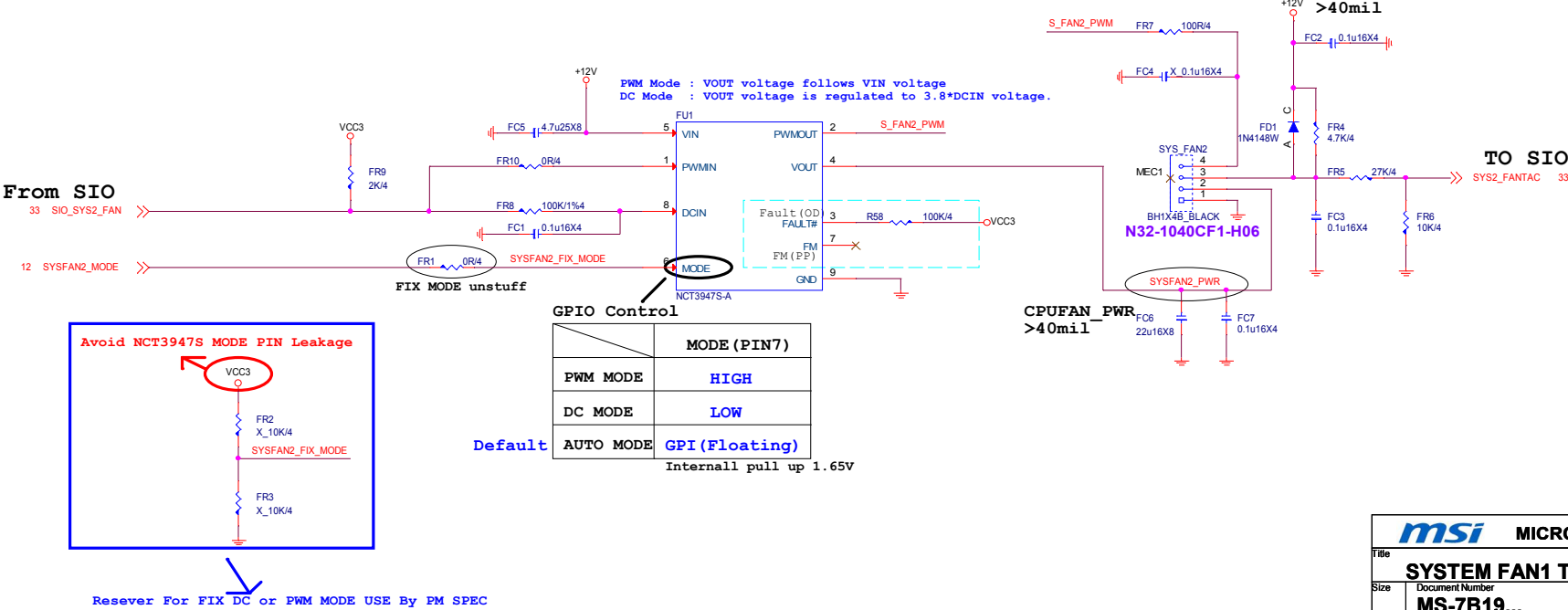


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

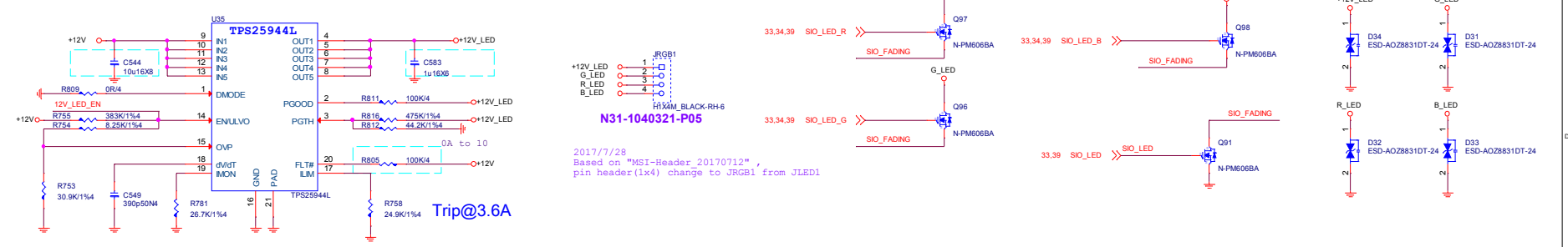
2.GPIO可以由BIOS切换 PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



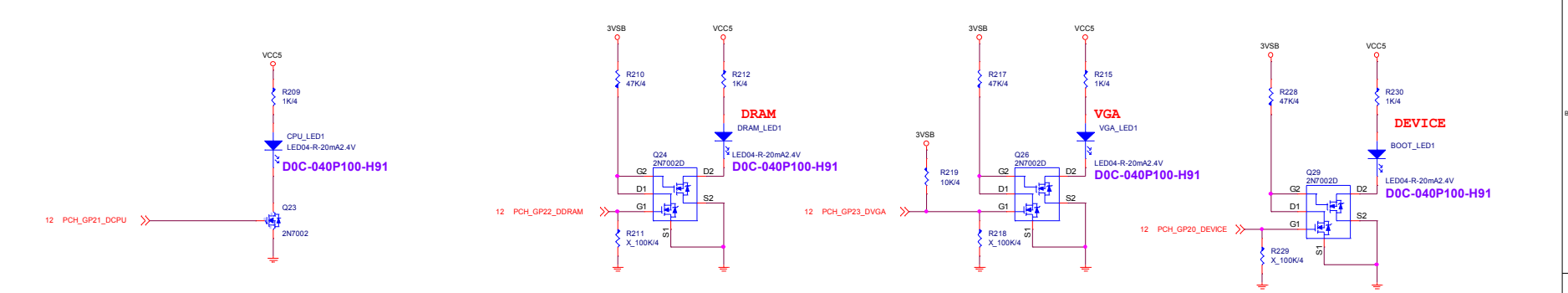
JLED



BOTTOM LED



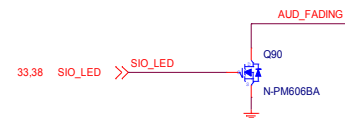
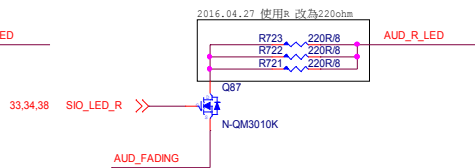
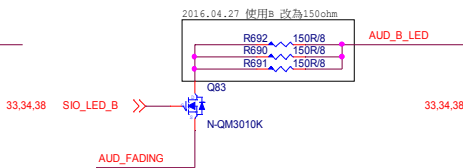
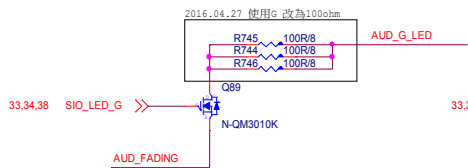
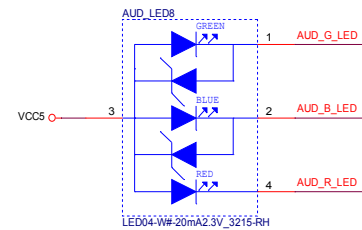
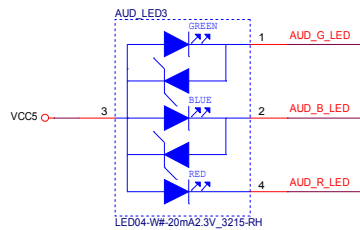
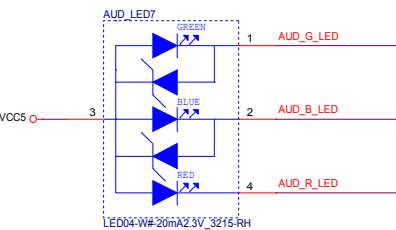
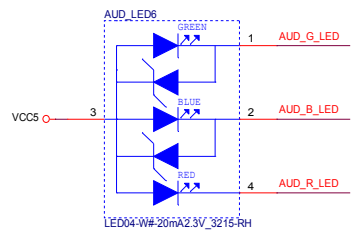
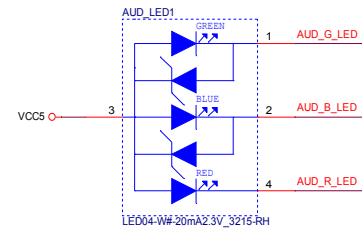
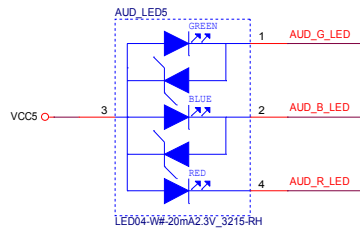
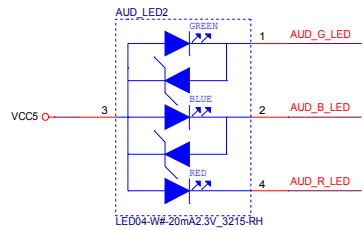
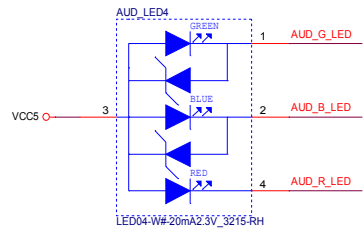
EZ DEBUG



GPIO LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
減	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

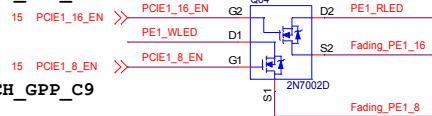
關機斷電狀態下，4個LED先維持default全暗，開機通電後：  
1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。  
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。  
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。  
4. 因此最後正常順利開機後，三個LED燈都是減掉的。  
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

**AUDIO\_LED**  
Audio moat is transparent and width 40mil

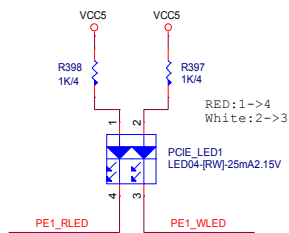
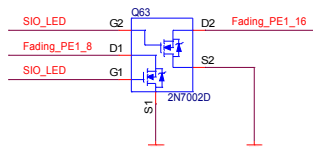


**PCIE1\_LED**

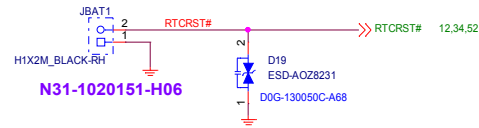
**PCH\_GPP\_C8**



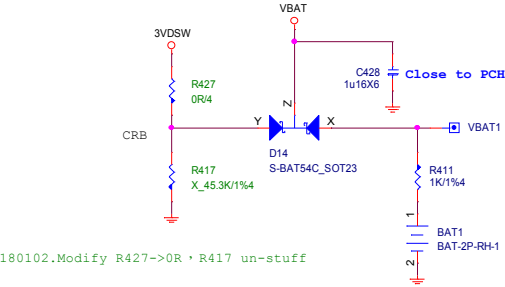
**PCH\_GPP\_C9**



CUT VBAT

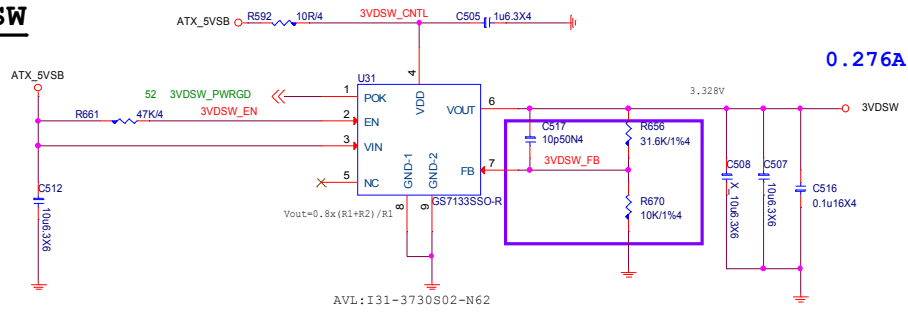


VBAT



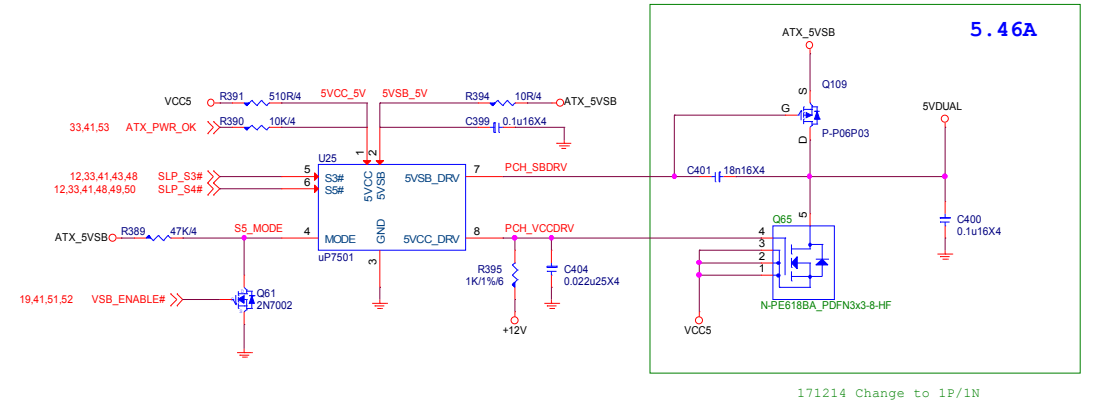
180102.Modify R427->0R , R417 un-stuff

## 3VDSW



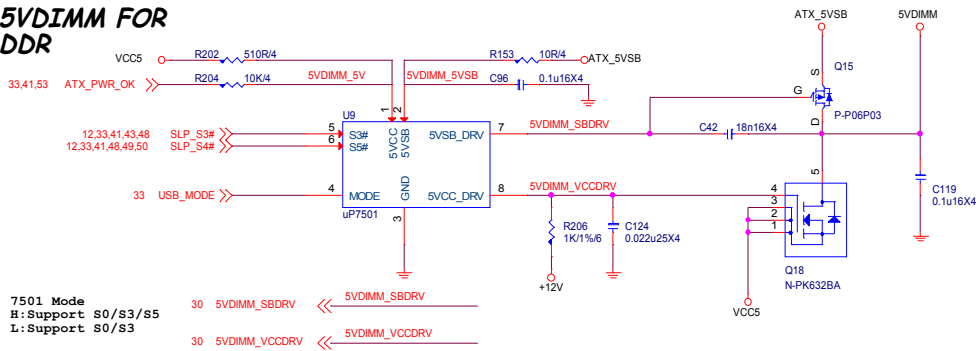
## 5VDUAL

5VDUAL is power source of 1P0SB

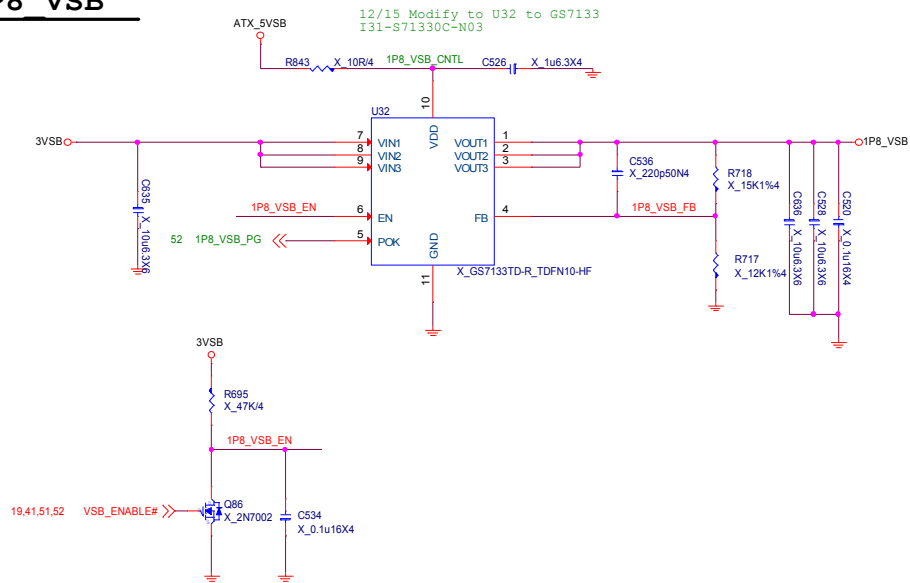


171211 Remove LDO Patch Circuit

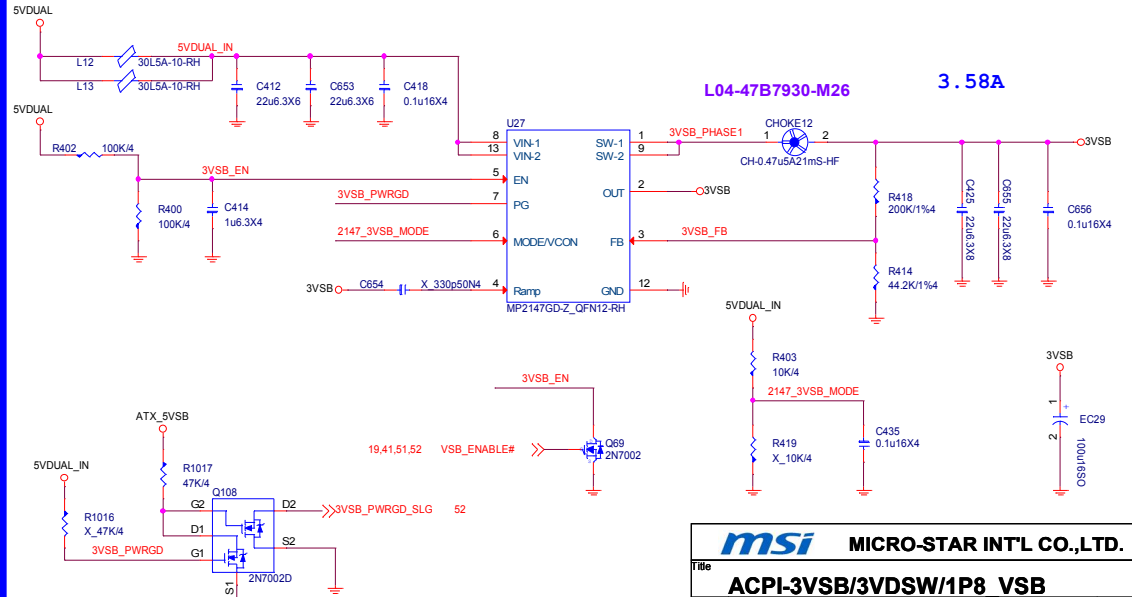
## 5VDIMM FOR DDR



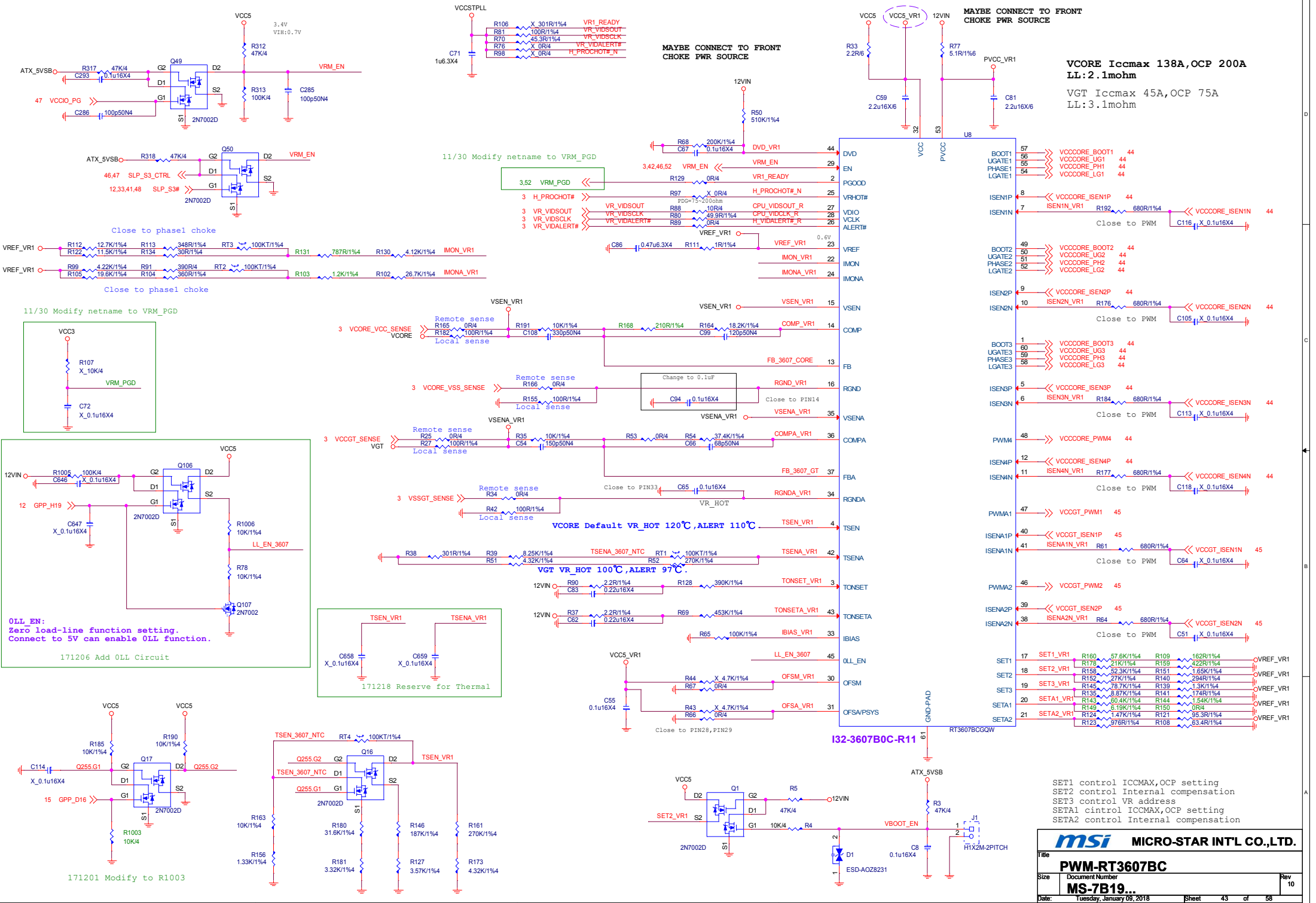
## 1P8 VSB



## 3VSB

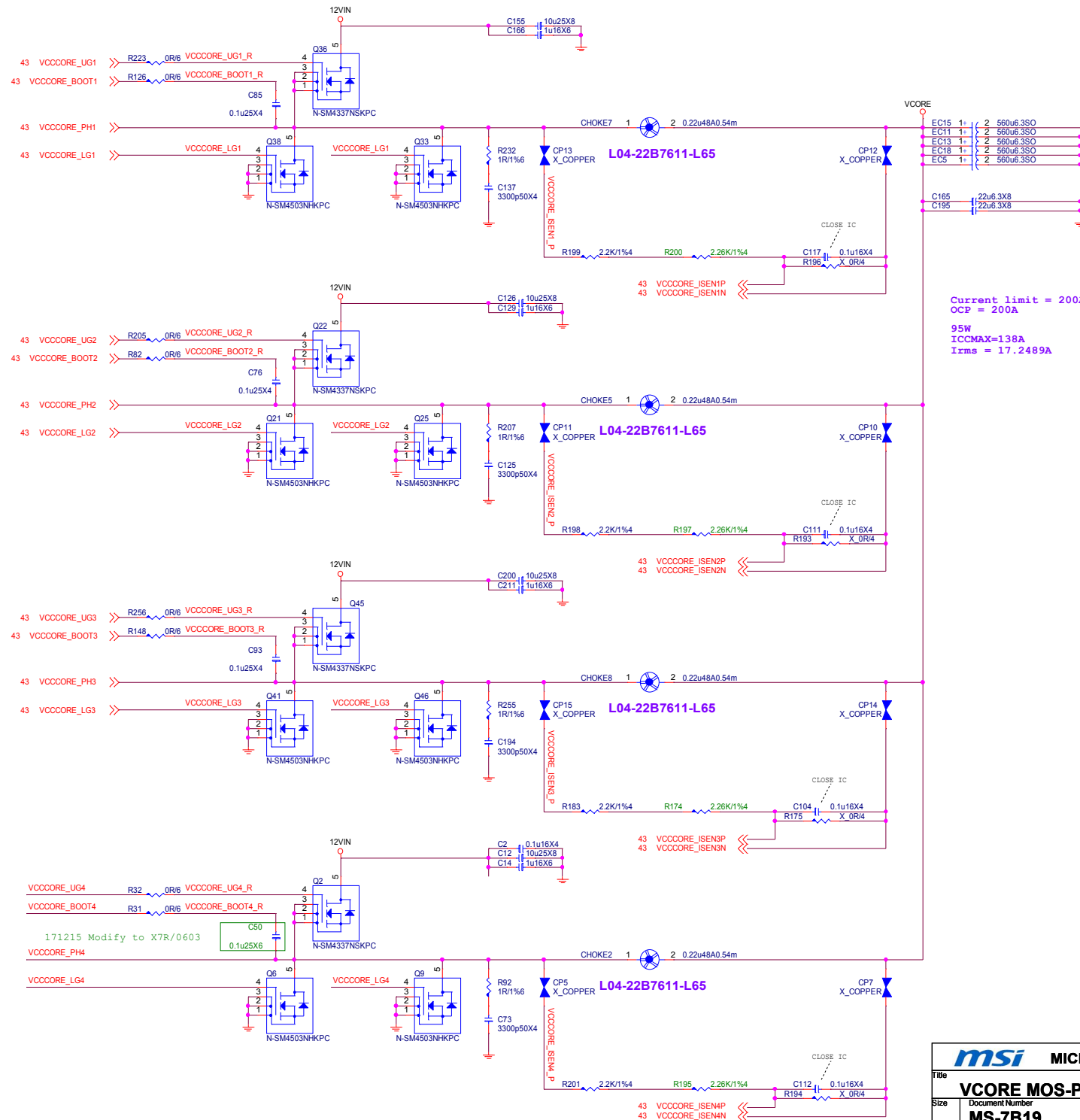






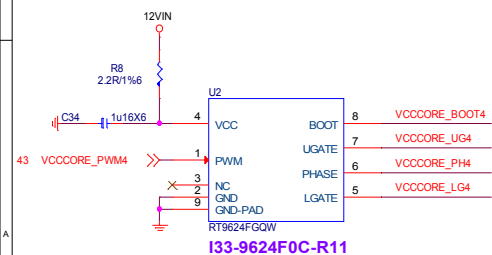
D03-4337N0C-ST8: 7.1 mohm

D03-4503N0C-ST8: 3 mohm



```
Current limit = 200A
OCP = 200A

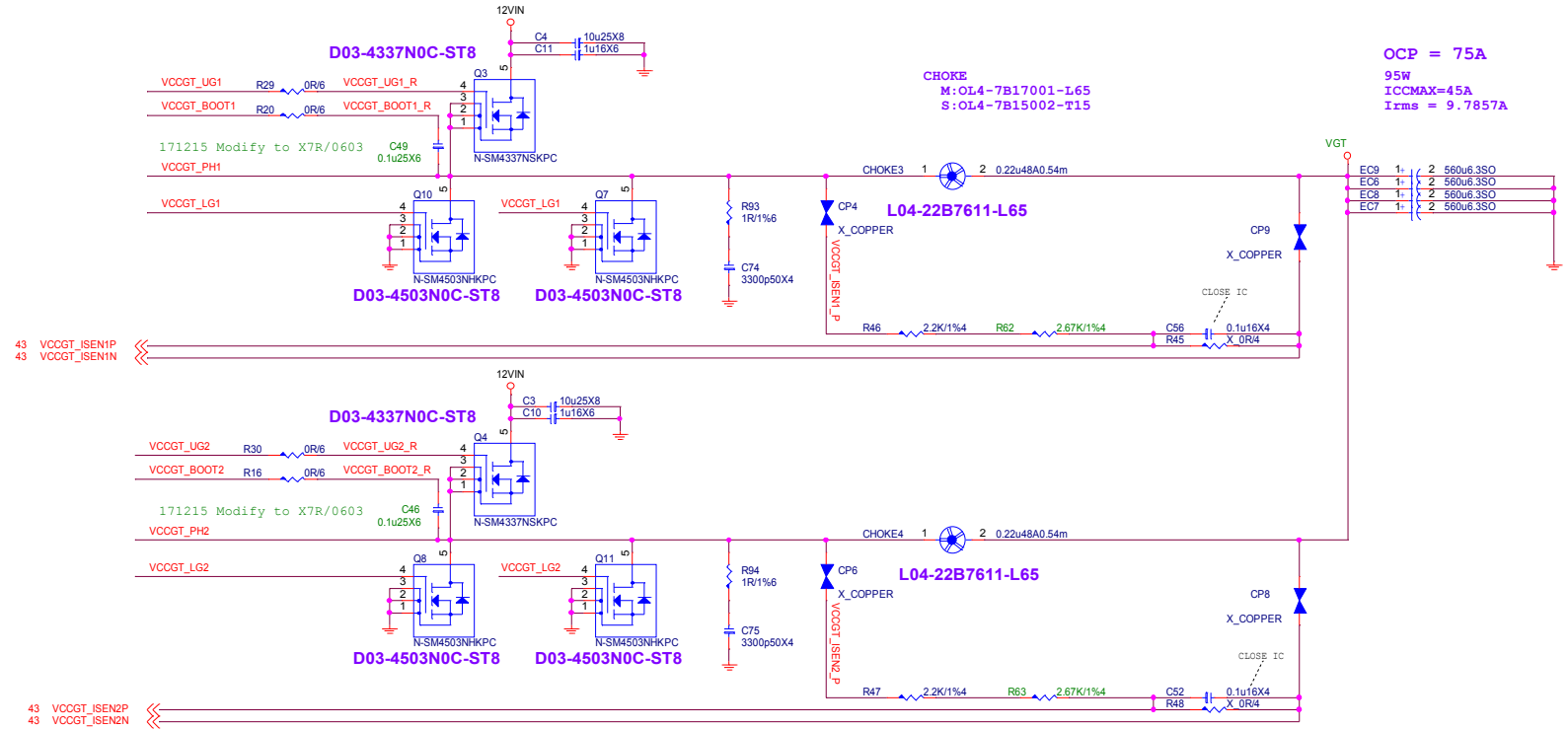
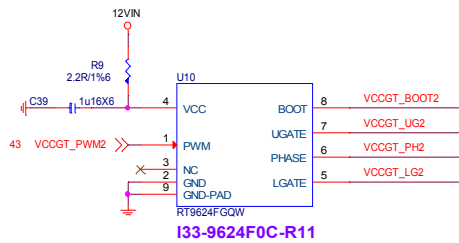
95W
ICCMAX=138A
Irms = 17.2489A
```



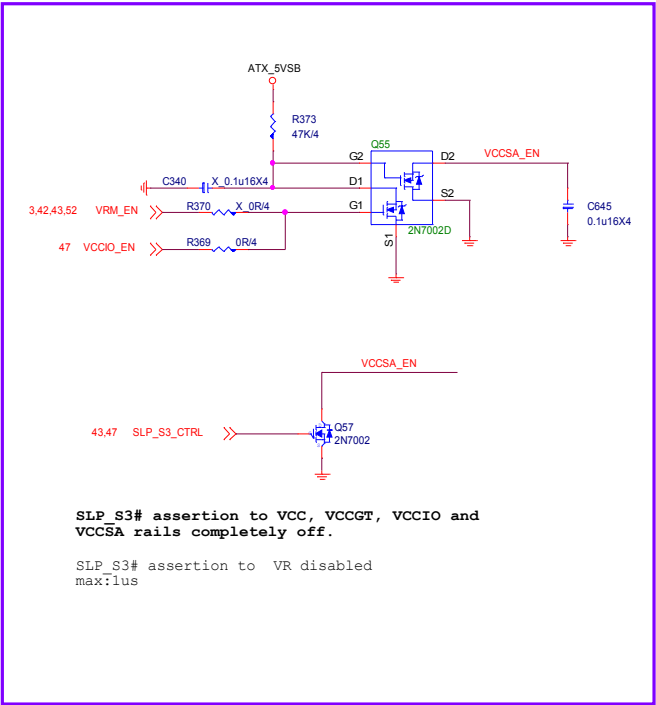


D03-4337N0C-ST8: 7.1 mohm

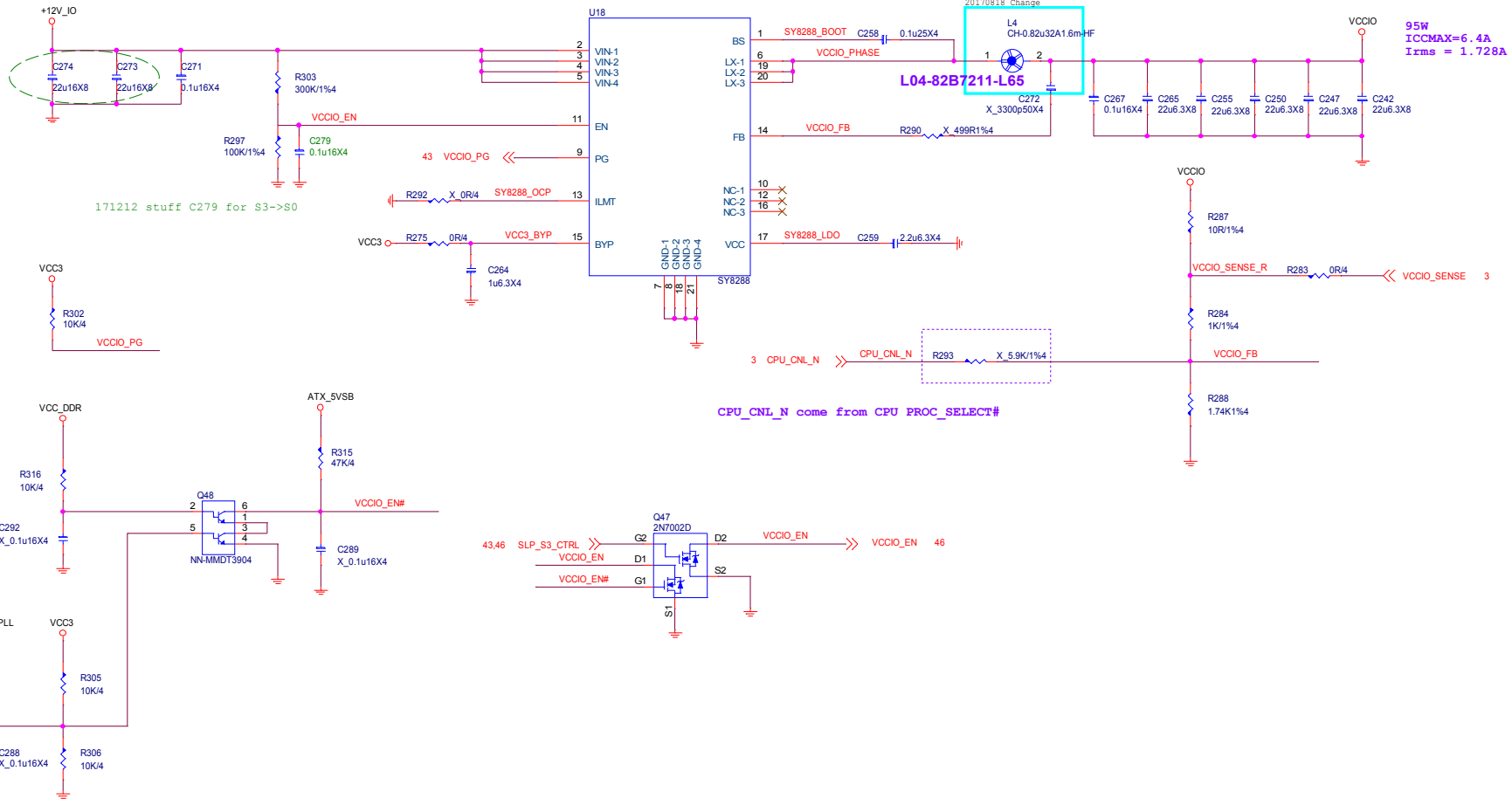
D03-4503N0C-ST8: 3 mohm



171201 update



IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.



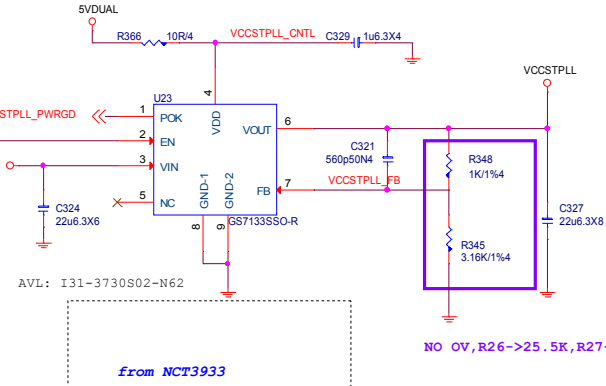
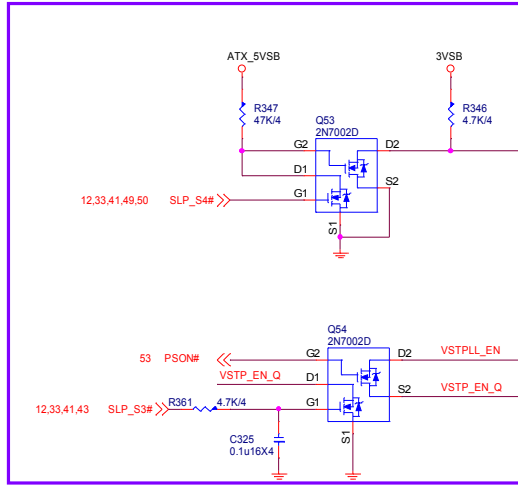
SY8288_OCP	OCP
0	8A
floating	12A
1	16A

# VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge

VCCST:80mA  
VCCPLL:150mA



NO OV,R26->25.5K,R27->100K, C178 unstuff

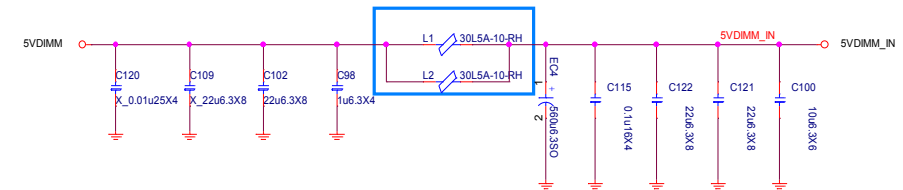
VCCIO ramped and stable before  
beginning of VCCOPC/VCCEPIO ramp

VCCST/PLL stable 1ms before PROC\_PWRGD

DDR4\_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU  
7.85A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

$I_{in} = 9.525A \times 1.2V / 0.8 / 5V = 2.8575A$   
L02-3008043-M26  
Over 85°C, Rated Current 1.5A.



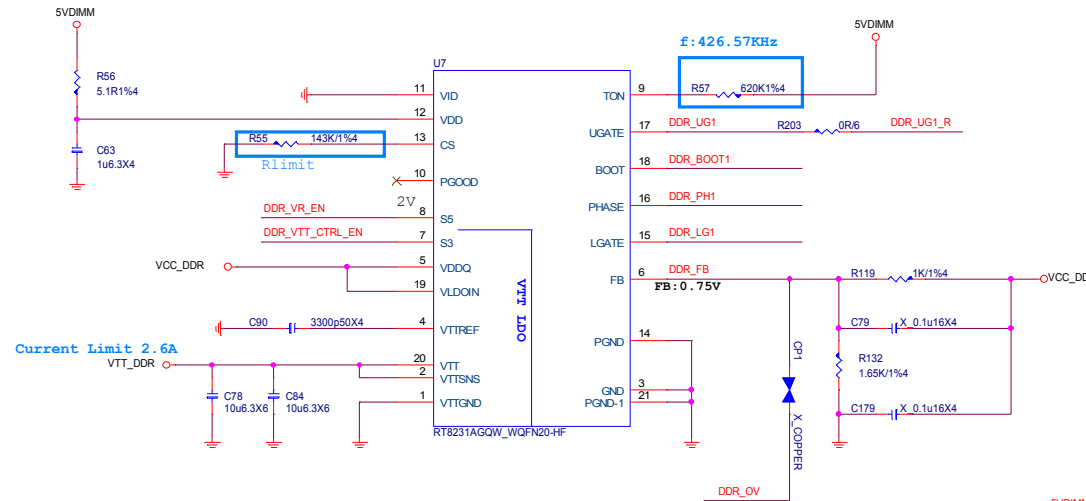
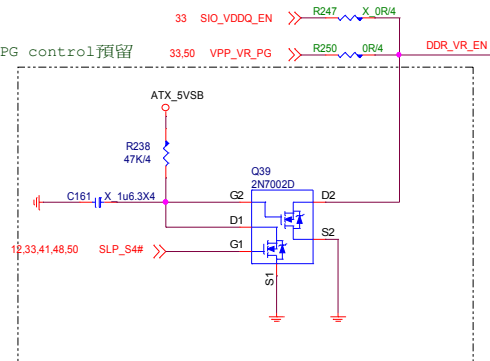
VID	Reference Voltage (V)
H	0.675
L	0.75

$$I_{rms} = I_{out} \times \sqrt{(V_{out}/V_{in}) \times (1 - (V_{out}/V_{in}))}$$
$$= 9.525 \times 0.427$$
$$= 4.06797A$$

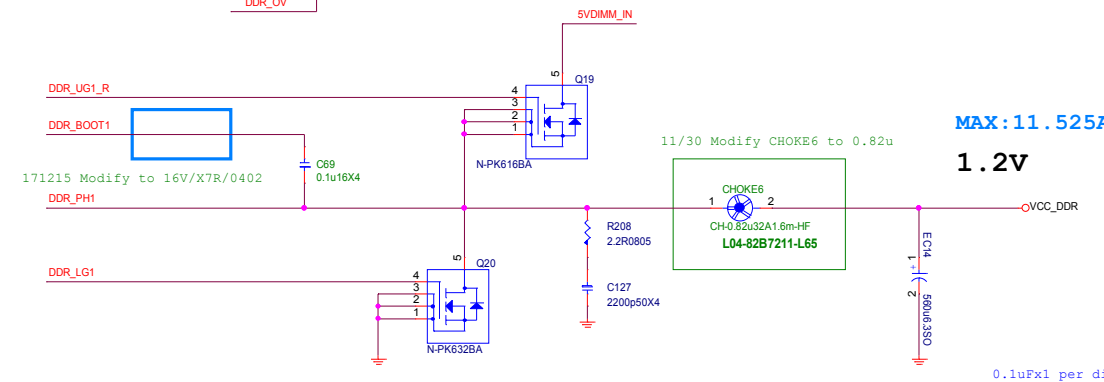
171219 Modify to VPP\_VR\_PG Control

From SIO pin 87

VPP\_VR\_PG control預留



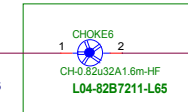
Current Limit 2.6A  
VTT\_DDR



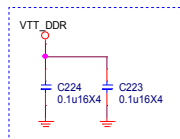
MAX: 11.525A

1.2V

11/30 Modify CH0KE6 to 0.82u

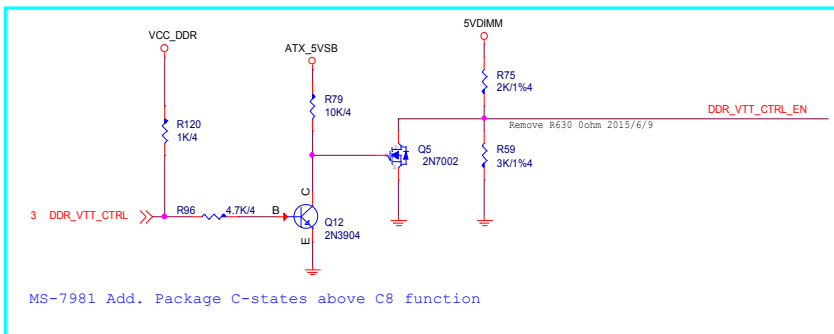


0.1uFx1 per dimm



SLP\_S4# de-assertion to VDDQ ramp down start

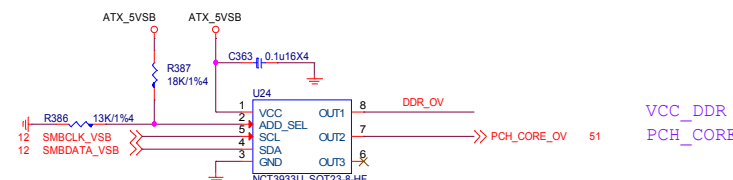
VPP ramp down after VDDQ ramp down



MS-7981 Add. Package C-states above C8 function

## UPI VOLTAGE CONSOLE

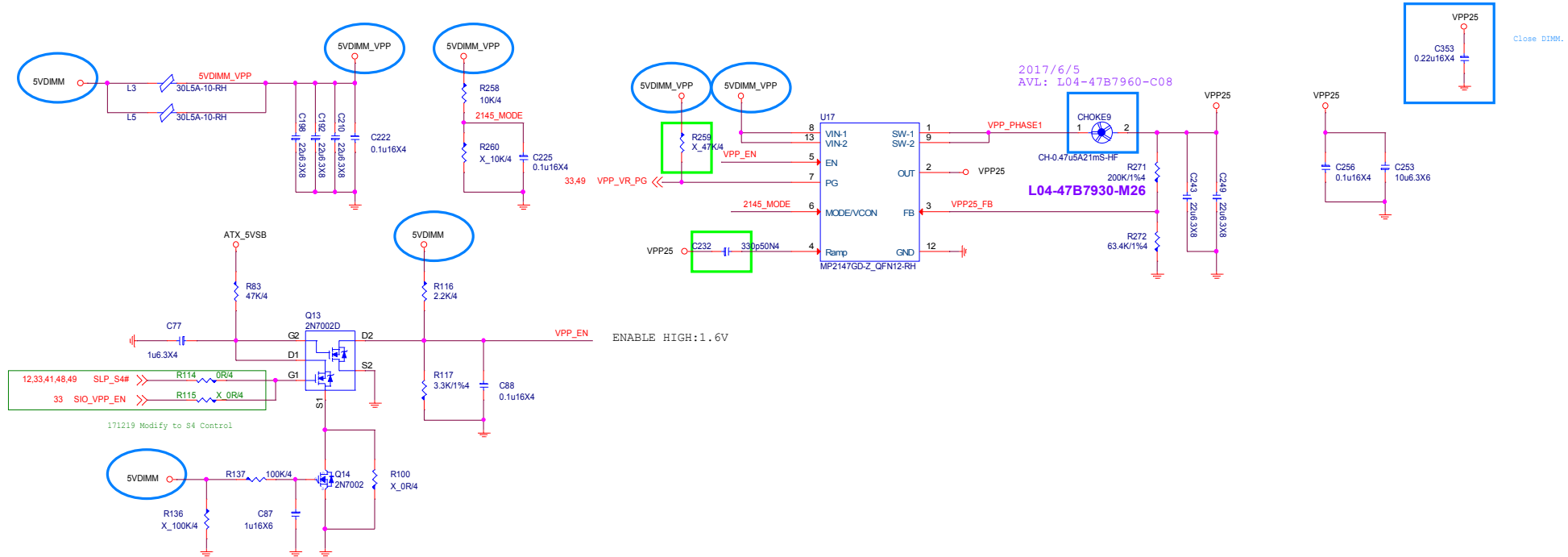
0x26: RH=18K, RL=13K



VCC\_DDR  
PCH\_CORE

4DIMM :2.24A FOR  
DDR VPP2.5V

# VPP25 Power 2.5V; 2.24A



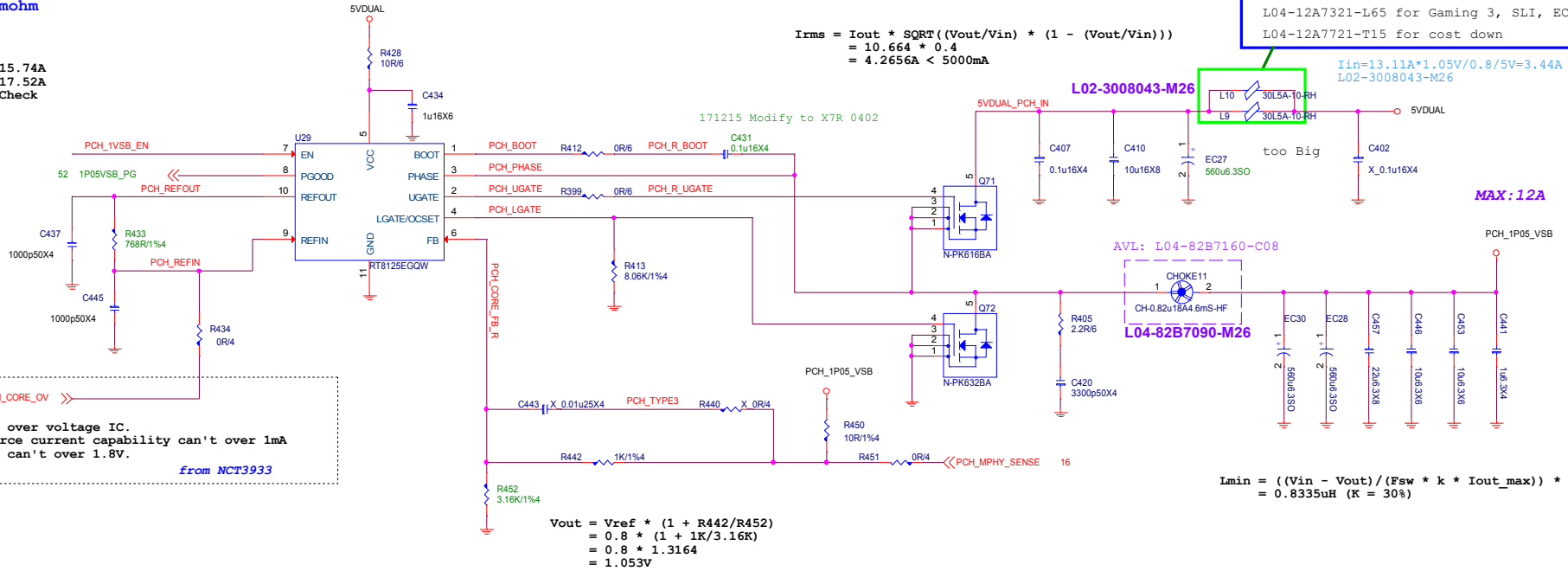
# PCH 1P05\_VSB

1.05V; 12A

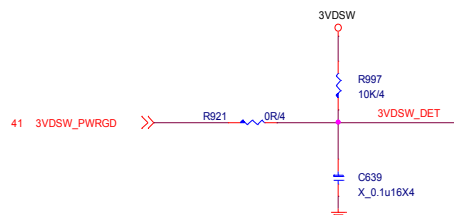
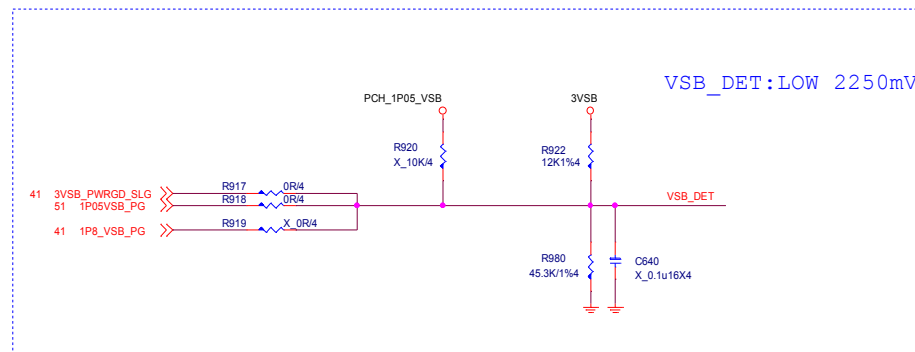
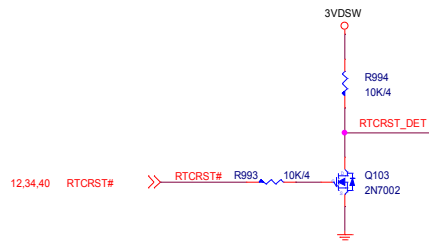
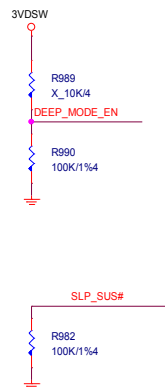
Rocpset:3.48K  
OCP=Rocset\*10uA/Rdson(Low side)  
=8.06K\*10uA/5.1mohm  
=15.8A

Rocs:8.06K,OCP:  
D03-4C05N03-O05 : 15.74A  
D03-632BA0C-N03 : 17.52A  
use UBIQ MOS need Check

Rdson (Low) 4.5V  
D03-3116M00-U47 : 3.6 mohm  
D03-632BA0C-N03 : 4.6mohm  
D03-3056M00-U47 : 6.2mohm

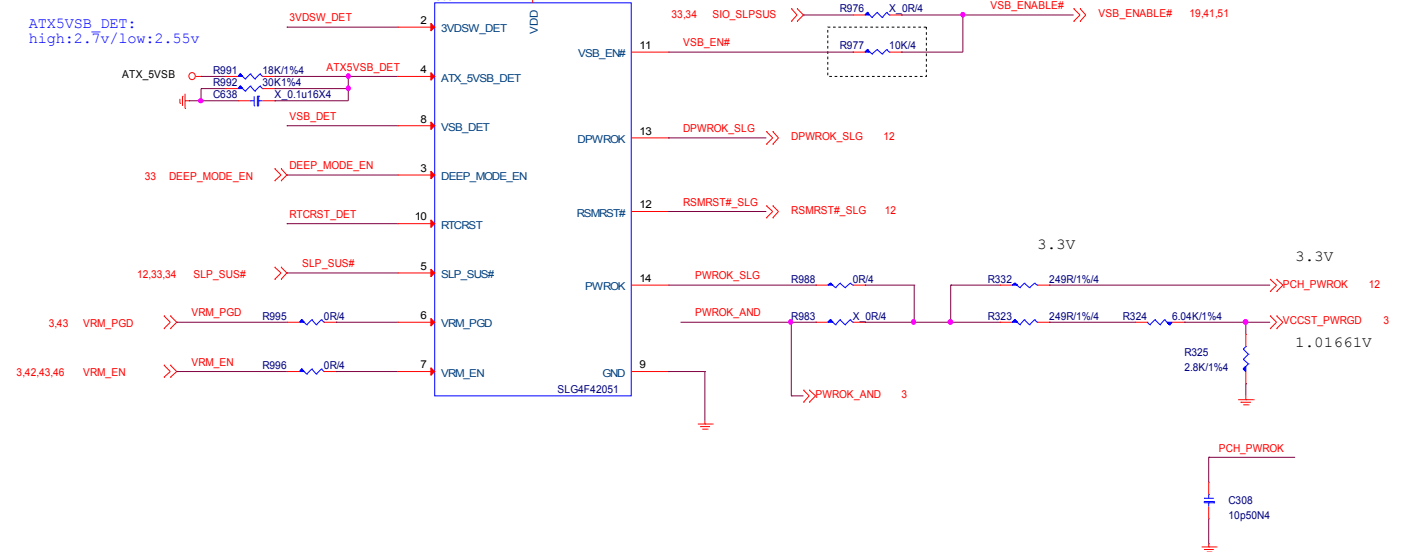


	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



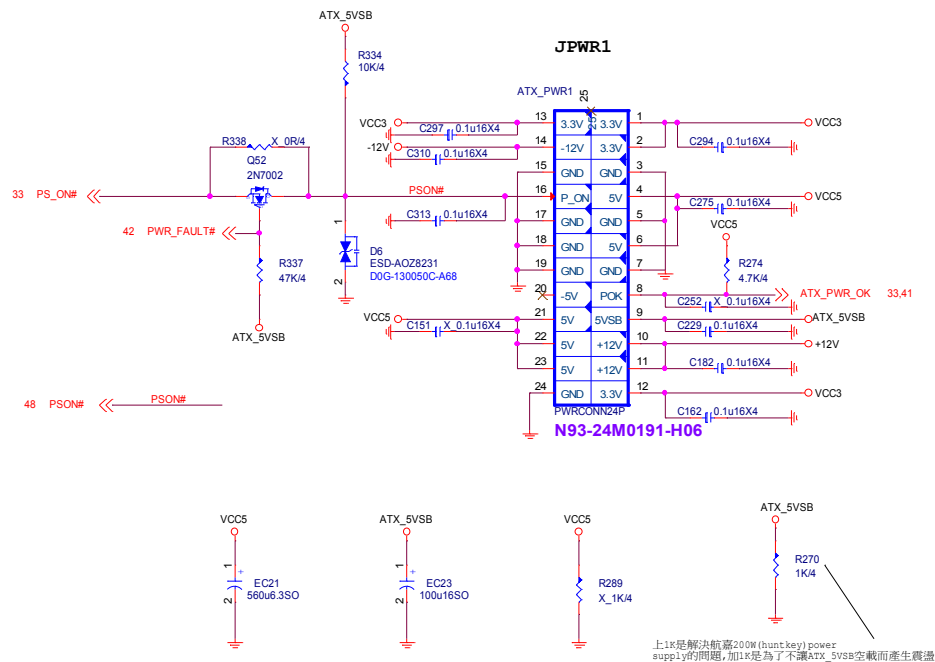
19 ATX5VSB\_DET

ATX5VSB\_DET:  
high:2.7v/low:2.55v

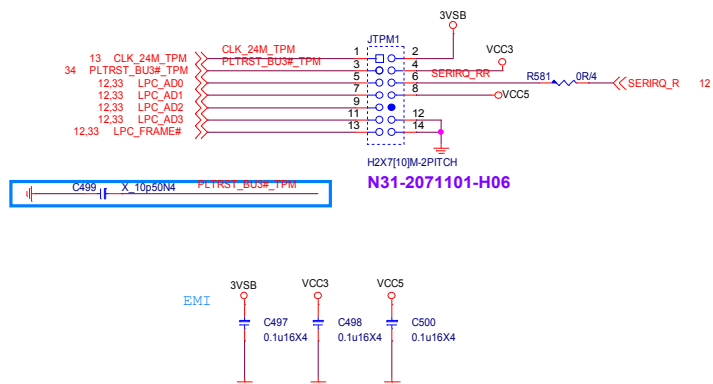




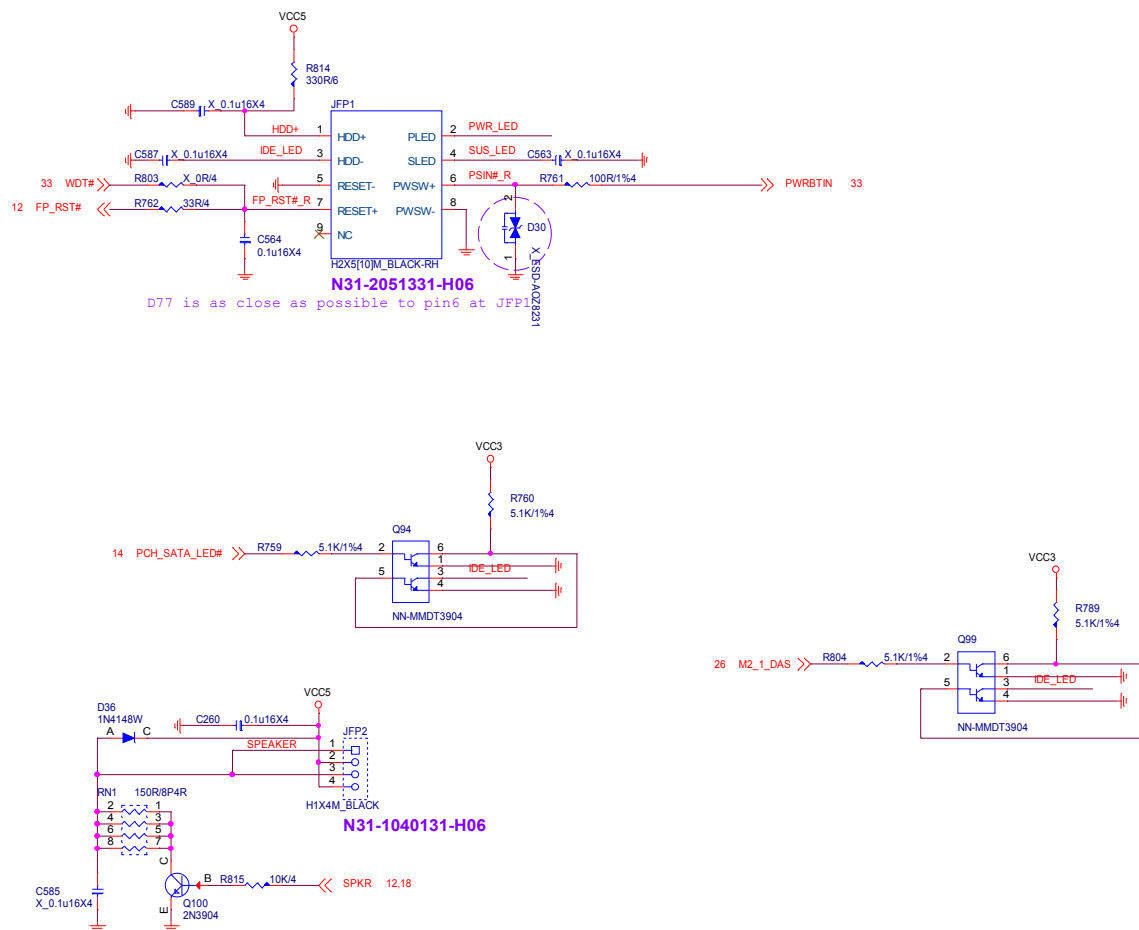
## ATX POWER CONNECTOR



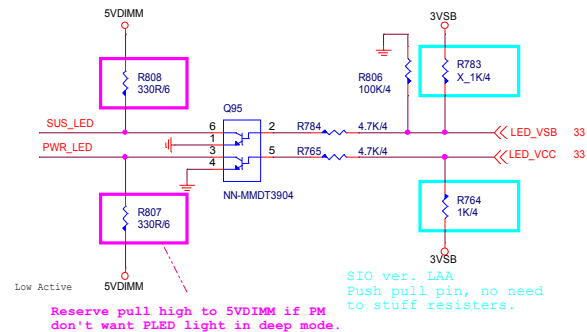
## TPM Pin Header



### FRONT PANNEL



## Front Panel





PD0-07B1910-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)  
PD0-07B1910-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



G51-M1SPXXA-A09



Y01-RHDMI03-000



Y02-MU00170-CFO



Y02-MA00101-SSE



Y02-MA00401-XSP



E21-7869020-F02



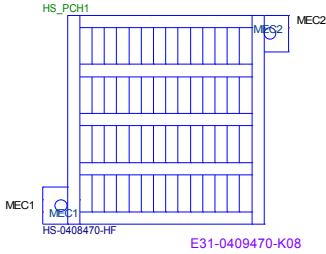
D06-0100101-P01



Y02-MU00100-NAH

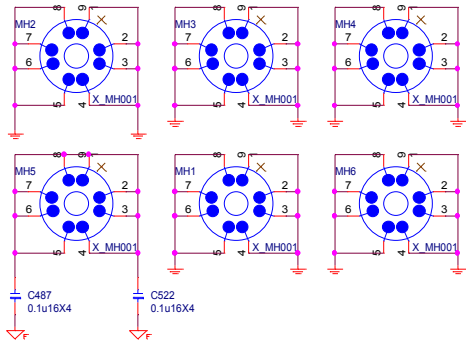


G51-M1SPM45-Q13

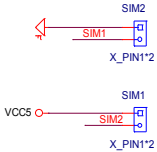


E31-0409470-K08

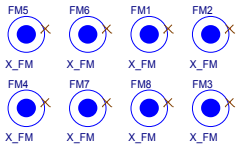
### Mounting Holes



### Simulation



### Optical Fiducial Marks-120



## Vcheck

PCH_1P05_VSB	○	—	■	PCH_1P05_VSB	VCORE	○	—	■	VCORE
VCCSTPLL	○	—	■	VCCSTPLL	VGT	○	—	■	VGT
VPP25	○	—	■	VPP25	VCC_DDR	○	—	■	VCC_DDR
1P8_VSB	○	—	■	1P8_VSB	VCCSA	○	—	■	VCCSA
3VSB	○	—	■	3VSB	VCCIO	○	—	■	VCCIO
3VDSW	○	—	■	3VDSW	VTT_DDR	○	—	■	VTT_DDR